
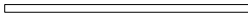

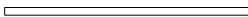


8S650GXM Schematics

Revision 1.0

SHEET	TITLE
1	COVER SHEET
2	BOM & PCB MODIFY HISTORY
3	BLOCK DIAGRAM
4,5,6	INTEL CPU_WMT_478
7-10	SIS651/645DX (NORTH BRIDGE) HOST; DDR; AGP,HYPER ZIP
11-14	962 (SOUTH BRIDGE)
15	CKG(ICS952004) + CKBF (ICS93722)
16,17	DDR SDRAM DIMMS 1,2 & DDR TERMINATION
18	AGP SLOT
19	VGA Connector
20	PCI SLOT 1-3
21	IDE,USB
22	Winbond W83697HF
23	BIOS
24	COM,PRT,FDD,KB/MS,IR
25	CNR SLOT
26	AUDIO AC 97 CODEC
27	AUDIO JACK,GAME PORT
28	RTL8100B & USB CONNECTOR
29	PANEL,STR LED,FANS ,CPU GN
30	VCORE PHASE PWM HIP 6301 + 6601
31	ALL POWER CIRCUIT
32	ATX & ATX12V CONN
33	GPIO Connection
34	TEST POINT

 COMPONENT SIDE (1 oz. Copper)	
 GND SIDE (1 oz. Copper)	
 VCC SIDE (1 oz. Copper)	
 SOLDER SIDE (1 oz. Copper)	
GIGABYTE	
Title: COVER SHEET	
Size: Custom	Document Number: GA-8S650GXM
Date: Wednesday, May 07, 2003	Rev: 1.0
Sheet 1 of 32	

Model Name: 8S650GXM

Version:1.0

Component value change history

AUTOBOM
2002/06/04

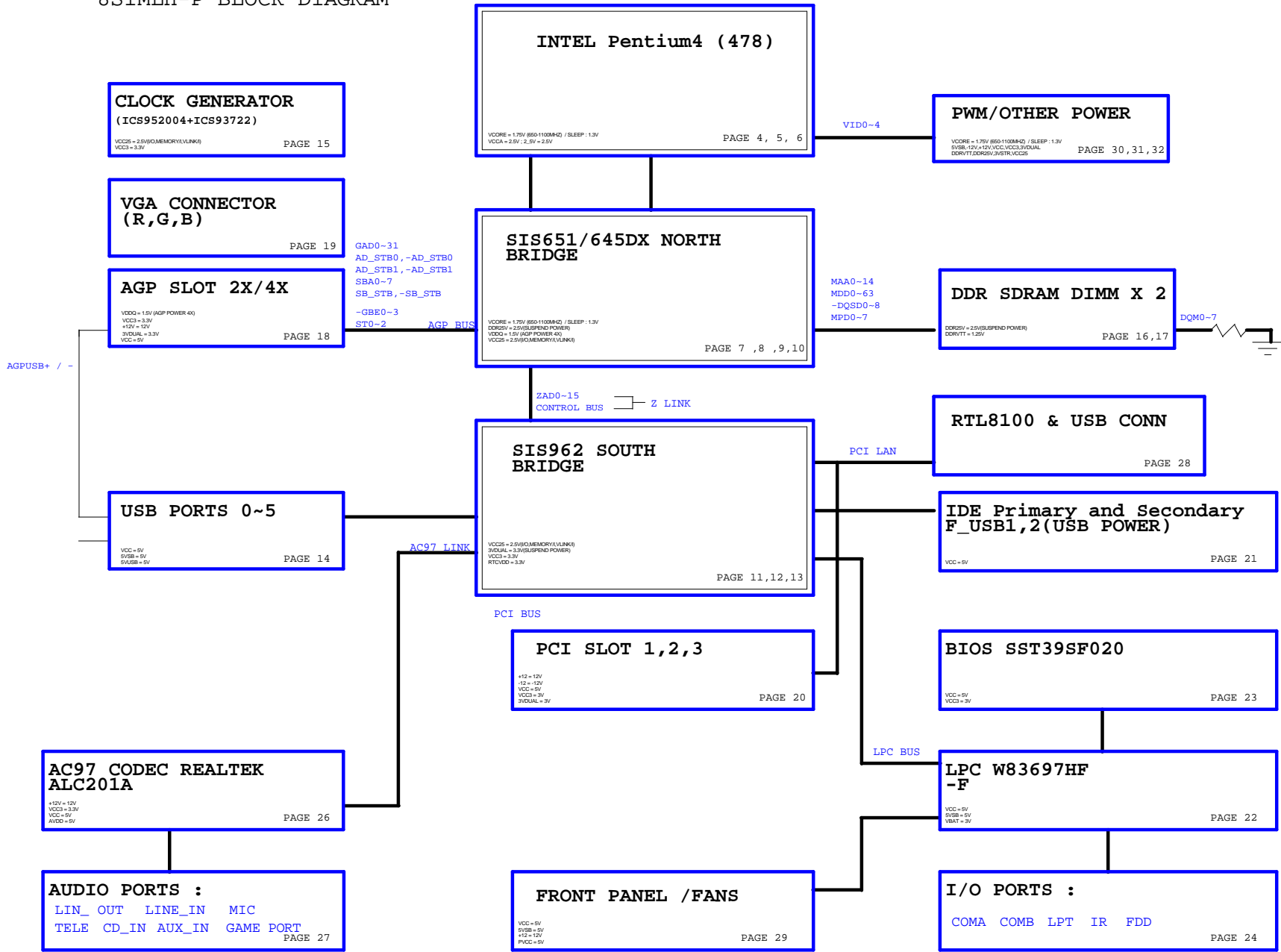
Date	Change Item	Reason
02/04	LAYOUT PLACEMENT	DEL 1394 CONNECTOR(LAYOUT ISSUE) SWAP NET
02/05	LAYOUT LIB	COIL-8P---->COIL-8P_SHORT
02/06	VGA/COM DUAL LAYOUT	
	DDRVTT (R&D 109)	DDRVTT DECOUPLING X14 PCS (0.1U/8P4C CAP)
02/06-1	LAYOUT LIB MODIFY	USB2.0 CHOKE (NO SHORT) AGP SLOT-->AGP_N
02/19	NET SWAP	BC345-->SC60(COMP-->SOLDER SIDE)
02/20	EMI ISSUE	CLOSE U16(75232) -NTXD2 ADD CAP 180P/6(BC349)
02/21	LAYOUT ISSUE	BC344-->SC61(COMP-->SOLDER SIDE) SWAP NET
	LIB MODIFY	MOSFET LIB TO263,252 CO LAYOUT(Q_TO263-252)
04/22	BOM MODIFY	AC97 CODEC --->ALC650
	PCB REV1.9	PWM 2 PHASE FAN5093M/C(VOCRE CAP COST DOWN) INTEL F_PANEL+F_USB1,2,F_AUDIO DDRVTT CAP 0.1U/8P4C X9PCS
04/23	PCB MODIFY	reduced PCB size(COST DOWN)
04/29		DEL MH6,ADD CAP MIC FOR EMI
05/08	PCB MODIFY	rename to GA-8SIMLH
	BOM MODIFY	SIS651+SIS962
05/13	BOM MODIFY	cost down CAP & FB ALC650 change to ST9721
05/21	PCB MODIFY	DEL BC218 ,ADD R1011 FOR F_MIC TEXT MODIFY
	BOM MODIFY	PCB CHANGE TO REV:2.0 1
06/04	BOM MODIFY	R867 10k/6 change to 470/6 R921 324/1/6 change to 487/1/6 ADD CN14,15,16,17 180P/8P4C ADD C944,C65 180P/N/50V/6
08/04	BOM MODIFY	IDE ,PANEL,USB FDD,SMBUS,22U TO 100U

Circuit or PCB layout change for next version

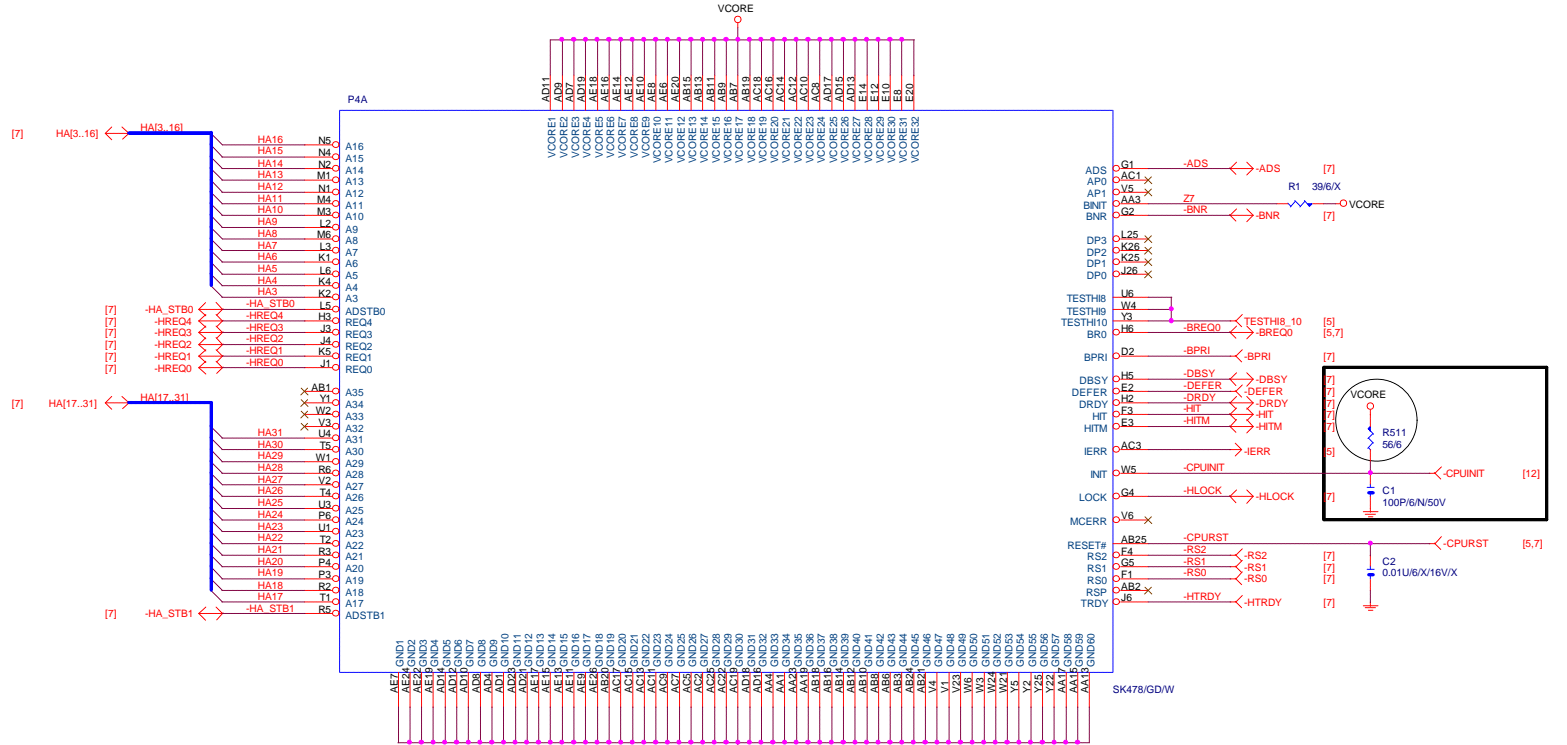
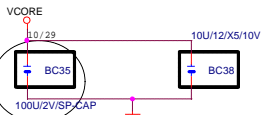
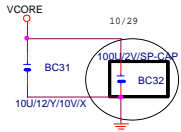
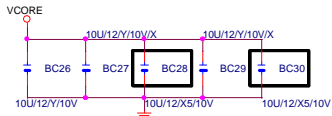
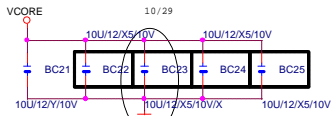
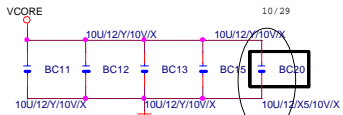
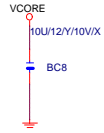
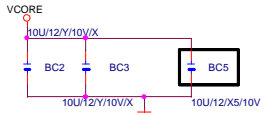
Date	Change Item	Reason
08/06	BOM MODIFY	U39 change to SIS962L REV:A2
08/12	BOM MODIFY	DEL R948 1K/6 ADD R950 470/6 R949 10/6 change to 22/6
08/13	BOM MODIFY	EC1,2,3,5,34,40,46 330U/25V change to 1200U/6.3V EC54 22U change to 100U
	BOM MODIFY	R939 200K/6 change to 240K/6 ST9721 change to ALC101
	PCB MODIFY	REV:2.01 CHANGE TO2.1
09/12	BOM MODIFY	EC37 100U change to 22U
10/14	BOM MODIFY	R935,R943 2.2 ohm Change to 4.7 ohm
10/28	BOM MODIFY	U12 ADD W83697HF/UB FOR MEMO change
11/15	PCB MODIFY	PCB size ADD 0.5 cm(SPEC change)
12/09	PCB MODIFY	PCB text modify
12/09	BOM MODIFY	DEL BC20,23 ADD BC21,BC26 10U/12 C110,C111 ADD 1K ohm C182 add 150 ohm R8 75/6/1 change to 100/6/1
		PCB change to REV:3.01
12/26	PCB MODIFY	ADD HT SUPPORT REV:3.02
01/03	PCB MODIFY	ADD HT SUPPORT REV:3.1
12/09	BOM MODIFY	R722,724,726 22 ohm change to 33 ohm U39 SIS962L/A2 change to SIS962L/C1 ADD C857 10P/6
02/12	PCB MODIFY	962L/C1 SUPPORT REV:3.2
02/24	PCB MODIFY	text modify
02/27	BOM MODIFY	PCB change to REV:3.21 AUDIO CHANGE TO ALC650
04/16	BOM MODIFY	FOR NOISE & EMI ISSUE FOR FAN5093/ C3
04/21	PCB MODIFY	CHANGE TO GA-8S650GXM
04/21	BOM MODIFY	SIS651 change to SIS650GX
05/07	BOM MODIFY	R722,R726 33 ohm change to 22 ohm , C855,C857 add 22P C859 10P change to 22P FOR EMI ISSUE

GIGABYTE			
BOM & PCB MODIFY HISTORY			
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Date:	Wednesday, May 07, 2003	Sheet	2 of 32

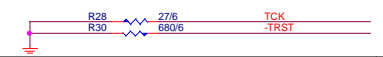
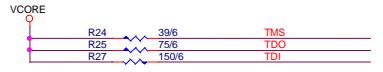
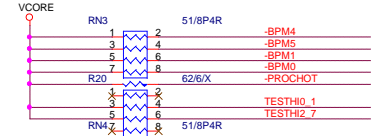
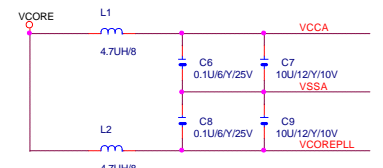
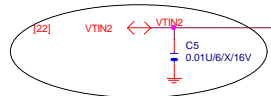
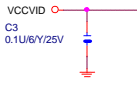
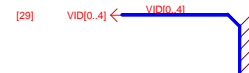
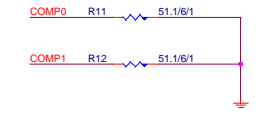
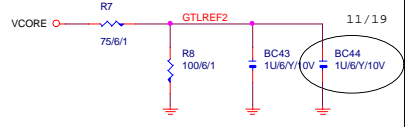
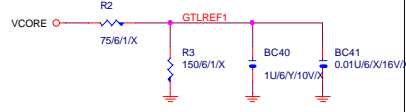
8SIMLH-P BLOCK DIAGRAM



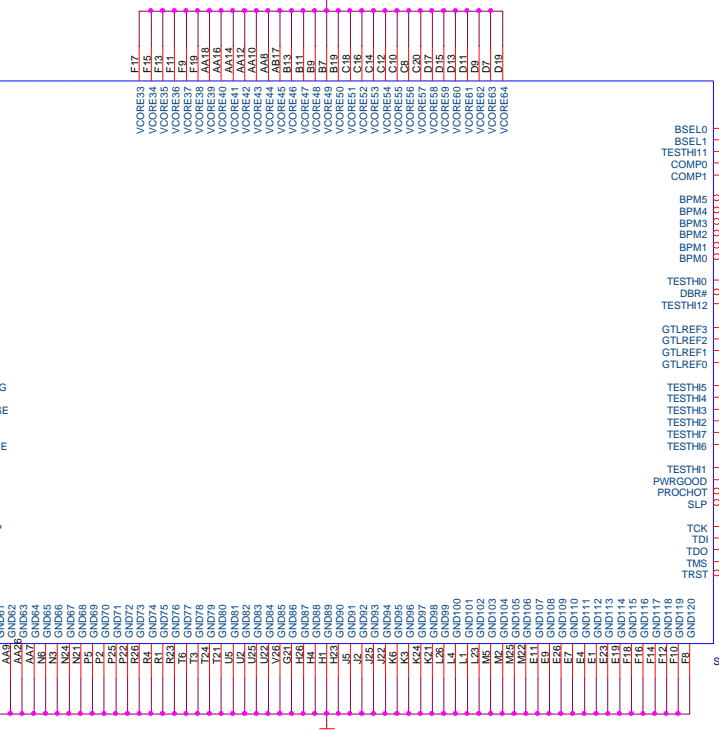
(X5R) X11 1206(10U) NOTE:GIGA



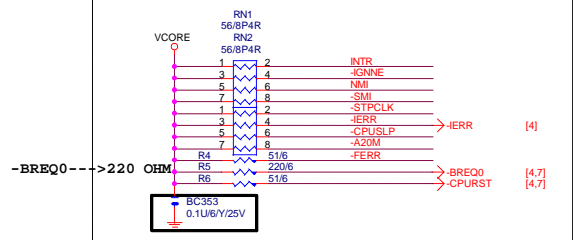
GIGABYTE			
WILLIAMATE 478A			
Size Custom	Document Number	GA-8S650GXM	
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			Rev 1.0



- [15] CPU_CLK CPU_CLK AF22 BCLK0
- [15] -CPU_CLK -CPU_CLK AC26 BCLK1
- [12] -A20M -A20M C6 A20M
- [12] -FERR -FERR B6 FERR
- [12] -IGNNE -IGNNE B2 IGNNE
- [12] INTR INTR D1 LINT0
- [12] NMI NMI E5 LINT1
- [12] -SMI -SMI B5 SMI
- [12] -STPCLK -STPCLK Y4 STPCLK
- [29] VID[0..4] VID0_4 AE1 VID4
- VID3 AE2 VID3
- VID2 AE3 VID2
- VID1 AE4 VID1
- VID0 AE5 VID0
- VCCVID AF4 VCCVID
- VCCA AF3 VCCVIDPRG
- AD20 VCCA
- VCC SENSE AS VCC_SENSE
- VCCIOPLL AE23 VCCIOPLL
- VSSA AD22 VSSA
- A4 VSS_SENSE
- AE21 RSVD1
- A22 RSVD2
- A7 RSVD3
- B3 THERMDA
- C4 THERMDC
- A2 THERMTRIP
- AD3 RSVD4
- AE25 RSVD5
- AD2 RSVD6
- AE24 RSVD7

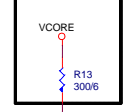


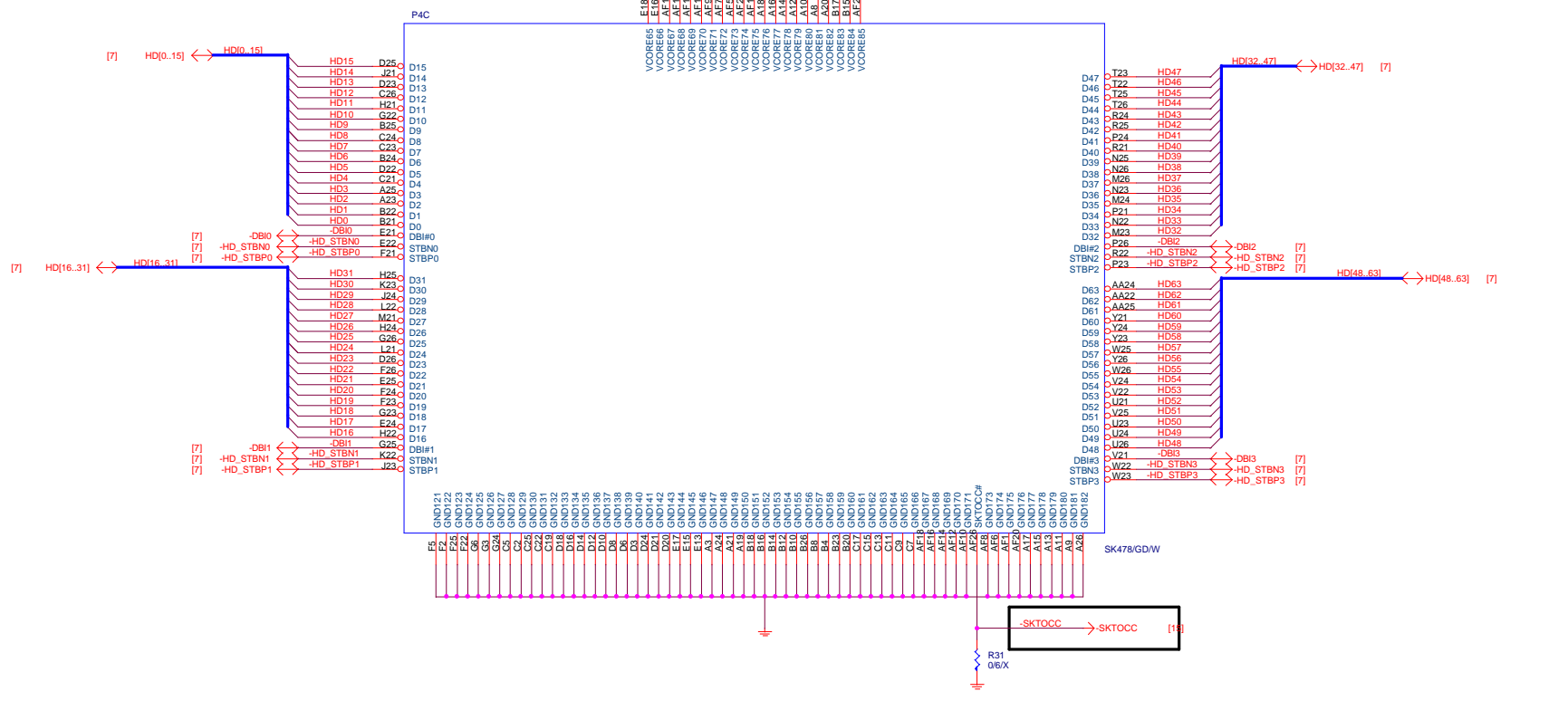
- AD6 BSEL0
- AD5 BSEL1
- A6 TESTH11
- L24 COMP0
- P1 COMP1
- AB4 -BPM5
- AA5 -BPM4
- Y6 -BPM3
- AC4 -BPM1
- AB5 -BPM0
- AC6 -BPM0
- AD24 TESTH0_1
- AE25 TESTH12
- AD25 TESTH12
- AA6 GTLREF1
- AA21 GTLREF2
- F20 GTLREF2
- AC23 TESTH5
- AC24 TESTH4
- AC20 TESTH3
- AC21 TESTH2
- AB22 TESTH7
- AA20 TESTH2_7
- AA2 TESTH0_1
- AB23 CPUPWOK
- C3 PROCHOT
- AB26 -CPUSLP
- D4 TCK
- C1 TDI
- D6 TDO
- E7 TMS
- E6 -TRST



BSEL0 --->100/133

SIS REQUEST





GIGABYTE			
WILLIAMATE 478C			
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Custom			
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-DBI0..31 <-> DBI0..31 [6]
 HDI0..63 <-> HDI0..63 [6]
 HAI3..31 <-> HAI3..31 [4]
 GDJ0..31 > GDJ0..31 [18]
 SBA0..71 > SBA0..71 [18]
 STI0..21 > STI0..21 [18]

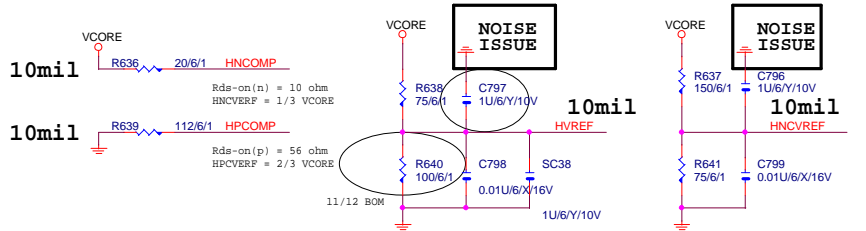
[15] HCLK <-> HCLK A126 CPUCCLK
 [15] HCLK <-> HCLK AH28 CPUCCLK#
 [4] HLOCK <-> HLOCK U24 HLOCK#
 [4] DEFER <-> DEFER U26 DEFER#
 [4] HTRDY <-> HTRDY V26 HTRDY#
 [4,5] CPURST <-> CPURST C20 CPURST#
 [5] CPUFWOK <-> CPUFWOK D19 CPUFWOK#
 [4] BPR1 <-> BPR1 T27 BPR#
 [4,5] BREQ0 <-> BREQ0 U25 BREQ0#
 [4] RS2 <-> RS2 T24 RS#2
 [4] RS1 <-> RS1 T26 RS#1
 [4] RS0 <-> RS0 U29 RS#0
 [4] ADS <-> ADS V28 ADS#
 [4] HITM <-> HITM U28 HITM#
 [4] HIT <-> HIT U28 HIT#
 [4] DRDY <-> DRDY W26 DRDY#
 [4] DBSY <-> DBSY V24 DBSY#
 [4] BNR <-> BNR V27 BNR#
 [4] HREQ4 <-> HREQ4 W28 HREQ#4
 [4] HREQ3 <-> HREQ3 W29 HREQ#3
 [4] HREQ2 <-> HREQ2 W24 HREQ#2
 [4] HREQ1 <-> HREQ1 W25 HREQ#1
 [4] HREQ0 <-> HREQ0 Y27 HREQ#0
 [4] HA_STB1 <-> HA_STB1 AD24 HASTB#1
 [4] HA_STB0 <-> HA_STB0 AA24 HASTB#0
 HA31 AF26C HA#31
 HA30 AE25C HA#30
 HA29 AH28C HA#29
 HA28 AD26C HA#28
 HA27 AG29C HA#27
 HA26 AE26C HA#26
 HA25 AF28C HA#25
 HA24 AC24C HA#24
 HA23 AG28C HA#23
 HA22 AE29C HA#22
 HA21 AD28C HA#21
 HA20 AC25C HA#20
 HA19 AD27C HA#19
 HA18 AE26C HA#18
 HA17 AF27C HA#17
 HA16 AB24C HA#16
 HA15 AB26C HA#15
 HA14 AC28C HA#14
 HA13 AC26C HA#13
 HA12 AC29C HA#12
 HA11 AA26C HA#11
 HA10 AB28C HA#10
 HA9 AB27C HA#9
 HA8 AA25C HA#8
 HA7 AA29C HA#7
 HA6 AA28C HA#6
 HA5 Y26C HA#5
 HA4 Y24C HA#4
 HA3 Y28C HA#3

HOST

651/645DX-1

AGP

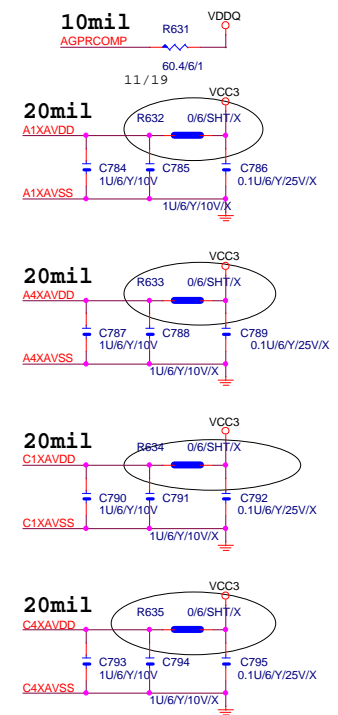
HDI#63 DBI#63
 HDI#62 DBI#62
 HDI#61 DBI#61
 HDI#60 DBI#60
 HDI#59 DBI#59
 HDI#58 DBI#58
 HDI#57 DBI#57
 HDI#56 DBI#56
 HDI#55 DBI#55
 HDI#54 DBI#54
 HDI#53 DBI#53
 HDI#52 DBI#52
 HDI#51 DBI#51
 HDI#50 DBI#50
 HDI#49 DBI#49
 HDI#48 DBI#48
 HDI#47 DBI#47
 HDI#46 DBI#46
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 HDI#32 DBI#32
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 HDI#22 DBI#22
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 HDI#19 DBI#19
 HDI#18 DBI#18
 HDI#17 DBI#17
 HDI#16 DBI#16
 HDI#15 DBI#15
 HDI#14 DBI#14
 HDI#13 DBI#13
 HDI#12 DBI#12
 HDI#11 DBI#11
 HDI#10 DBI#10
 HDI#9 DBI#9
 HDI#8 DBI#8
 HDI#7 DBI#7
 HDI#6 DBI#6
 HDI#5 DBI#5
 HDI#4 DBI#4
 HDI#3 DBI#3
 HDI#2 DBI#2
 HDI#1 DBI#1
 HDI#0 DBI#0



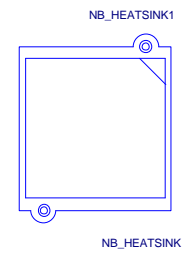
VREF C-CAP PULL-UP MEASURE NOISE WORST.

U38A

AC/BE#0 <-> GBE3 [18]
 AC/BE#1 <-> GBE2 [18]
 AC/BE#2 <-> GBE1 [18]
 AC/BE#3 <-> GBE0 [18]
 AREQ# <-> GREQ [18]
 AGNT# <-> GGNT [18]
 AFRAME# <-> GFRAME [18]
 AIRDY# <-> GIRDY [18]
 ATRDY# <-> GTRDY [18]
 ADEVSEL# <-> GDEVSEL [18]
 ASERR# <-> GSERR [18]
 ASTOP# <-> GSTOP [18]
 APAR <-> GPAR [18]
 RBF# <-> RBF [18]
 WBF# <-> WBF [18]
 PIPE# <-> PIPE [18]
 AGP8XDET <-> TP8 [18]
 ADIB# <-> TP9 [18]
 ADIBL <-> TP10 [18]
 SB_STB <-> SB_STB [18]
 SB_STB# <-> SB_STB# [18]
 AD_STB0 <-> AD_STB0 [18]
 AD_STB#0 <-> AD_STB#0 [18]
 AD_STB1 <-> AD_STB1 [18]
 AD_STB#1 <-> AD_STB#1 [18]
 GCLK_NB <-> GCLK_NB [15]
 AGRPCOMP <-> AGRPCOMP [18]
 A1XAVDD <-> A1XAVDD [18]
 A1XAVSS <-> A1XAVSS [18]
 A4XAVDD <-> A4XAVDD [18]
 A4XAVSS <-> A4XAVSS [18]
 AGPVREF <-> AGPVREF [18]
 AGPVSSREF <-> AGPVSSREF [18]
 HDSTBN#3 <-> HD_STBN3 [6]
 HDSTBN#2 <-> HD_STBN2 [6]
 HDSTBN#1 <-> HD_STBN1 [6]
 HDSTBN#0 <-> HD_STBN0 [6]
 HDSTBP#3 <-> HD_STBP3 [6]
 HDSTBP#2 <-> HD_STBP2 [6]
 HDSTBP#1 <-> HD_STBP1 [6]
 HDSTBP#0 <-> HD_STBP0 [6]



N.B HEATSINK



GIGABYTE		
SIS651/645DX(HOST/AGP)		
Title		
Size	Document Number	Rev
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MDDI[0:63] ↔ MDD[0:63] [16,17]
 DQM[0..7] → DQM[0..7] [16,17]
 MAA[0..14] → MAA[0..14] [16,17]
 -CS[0..3] → -CS[0..3] [16,17]
 -CKE[0..5] → -CKE[0..5] [16]
 -DQSDI[0..7] → -DQSD[0..7] [16,17]

11/19
short pad

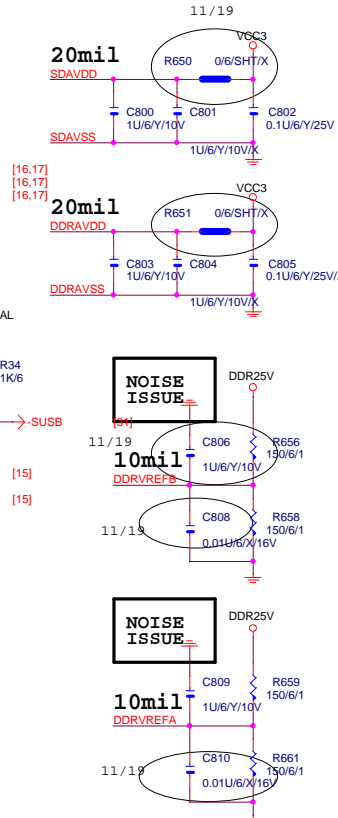
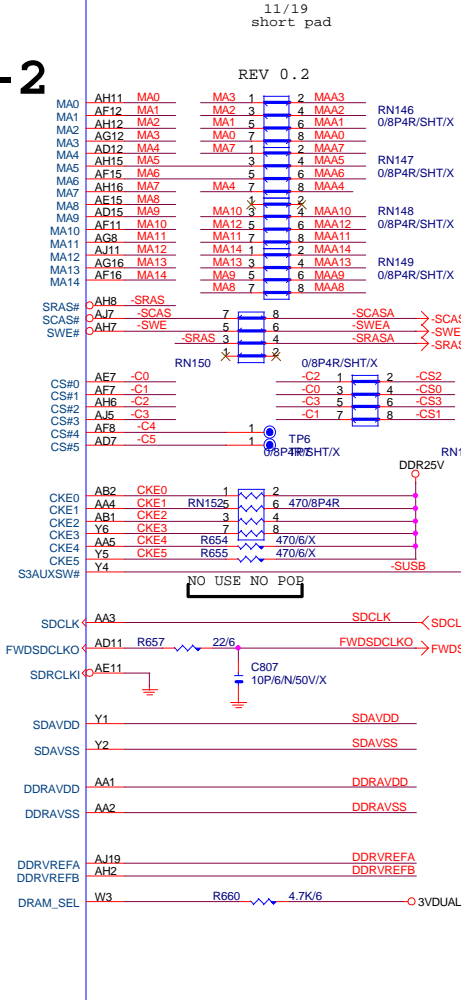
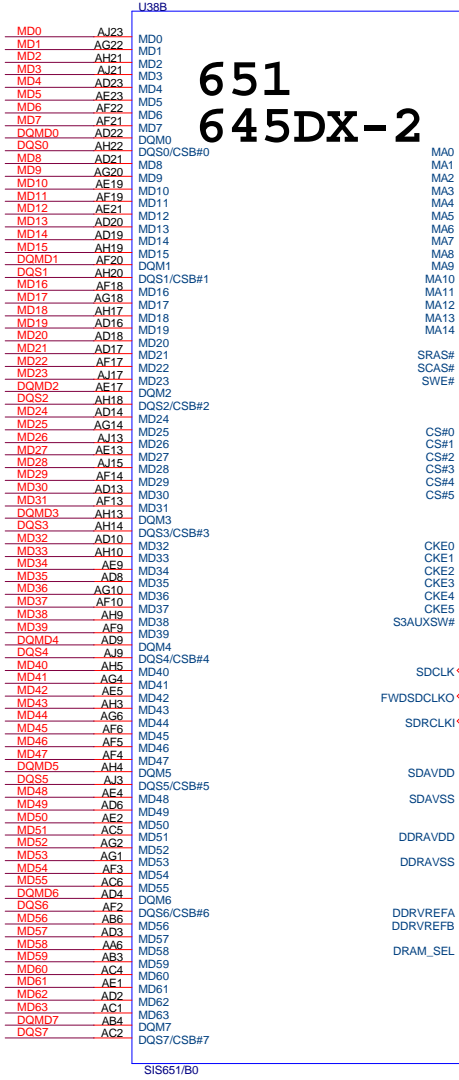
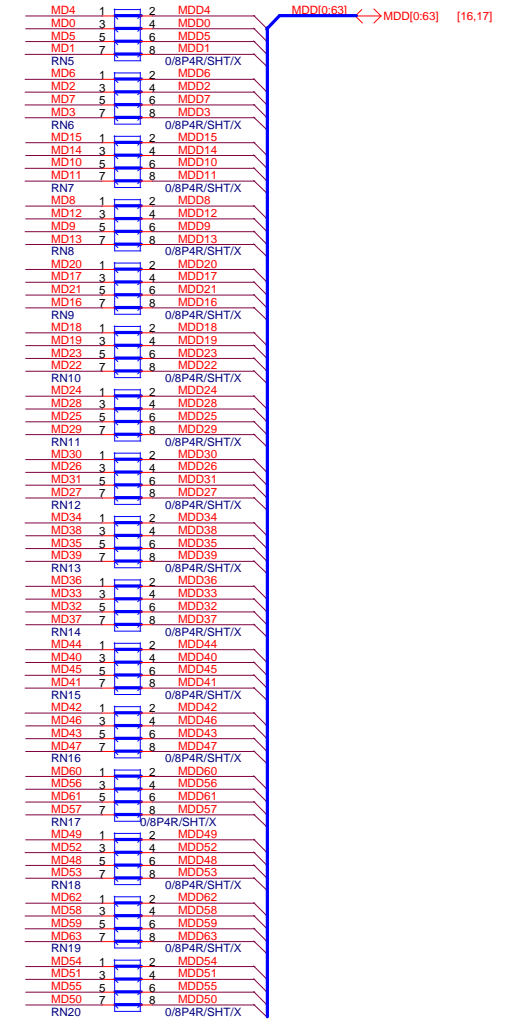
DDR MD DAMPING

Near DIMM 1

11/19
short pad

DQM0 R642 0/SHT/X DQMD0
 DQM1 R643 0/SHT/X DQMD1
 DQM2 R644 0/SHT/X DQMD2
 DQM3 R645 0/SHT/X DQMD3
 DQM4 R646 0/SHT/X DQMD4
 DQM5 R647 0/SHT/X DQMD5
 DQM6 R648 0/SHT/X DQMD6
 DQM7 R649 0/SHT/X DQMD7

DQS0 R40 0/SHT/X -DQSD0
 DQS1 R41 0/SHT/X -DQSD1
 DQS2 R42 0/SHT/X -DQSD2
 DQS3 R43 0/SHT/X -DQSD3
 DQS4 R44 0/SHT/X -DQSD4
 DQS5 R45 0/SHT/X -DQSD5
 DQS6 R46 0/SHT/X -DQSD6
 DQS7 R47 0/SHT/X -DQSD7



VREF C-CAP PULL-UP MEASURE NOISE WORST.

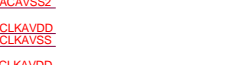
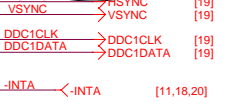
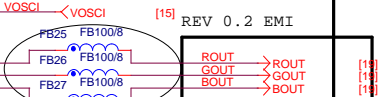
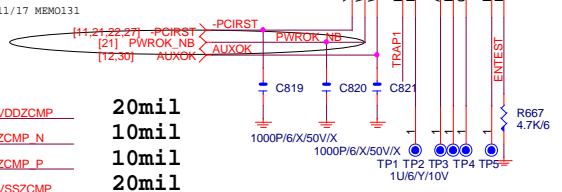
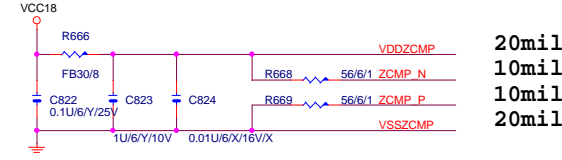
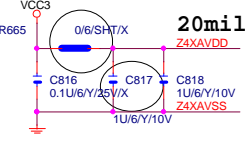
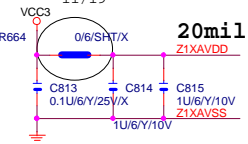
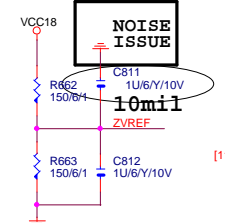
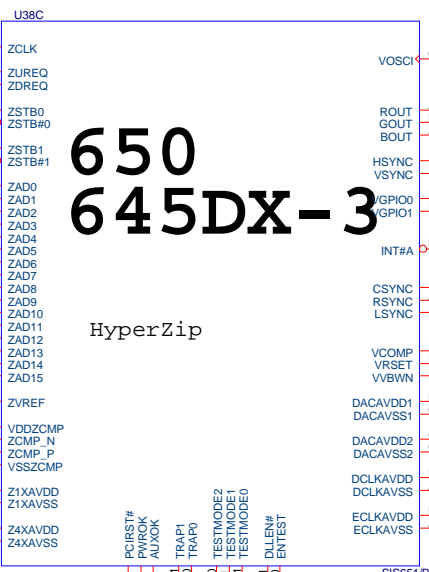
GIGABYTE		
Title SIS651/645DX(DDR)		
Size Custom	Document Number GA-8S650GXM	Rev 1.0
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NB Hardware Trap Table

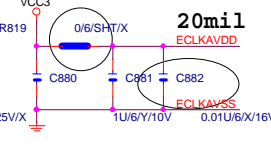
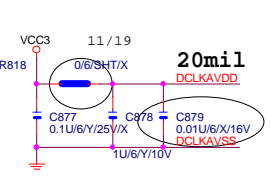
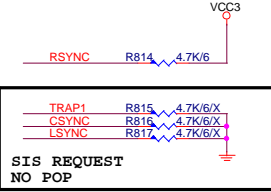
	0	1	Default	embedded pull-low (30-50K Ohm)
DLEN#	enable PLL	disable PLL	0	yes
DRAM_SEL	SDR	DDR	1(DDR)	yes
TRAP0	normal	NB debug mode	0	yes
TRAP1	TV selection, NTSC/PAL(0/1)		0	
CSYNC	enable VB		0	
RSYNC	enable VGA interrupt		1	
LSYNC	enable panel link		0	

650 645DX-3

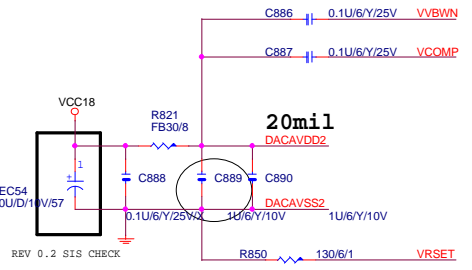
HyperZip



SIS 645DX NO POP



DACAVDD1 (VSS) -----> DACAVDD2 (VSS) (SIS AP-02)

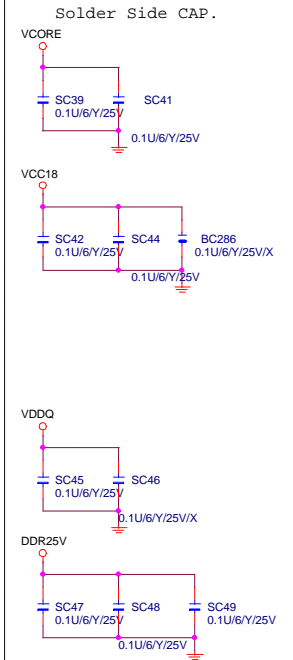
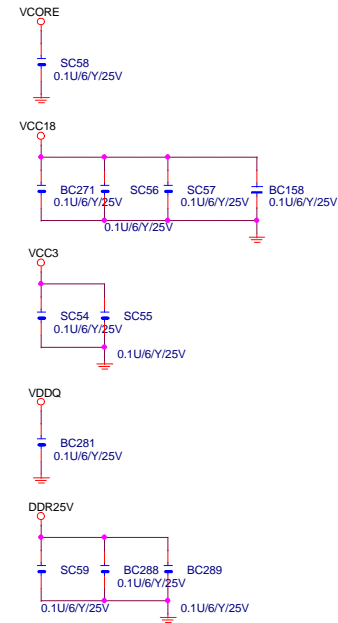
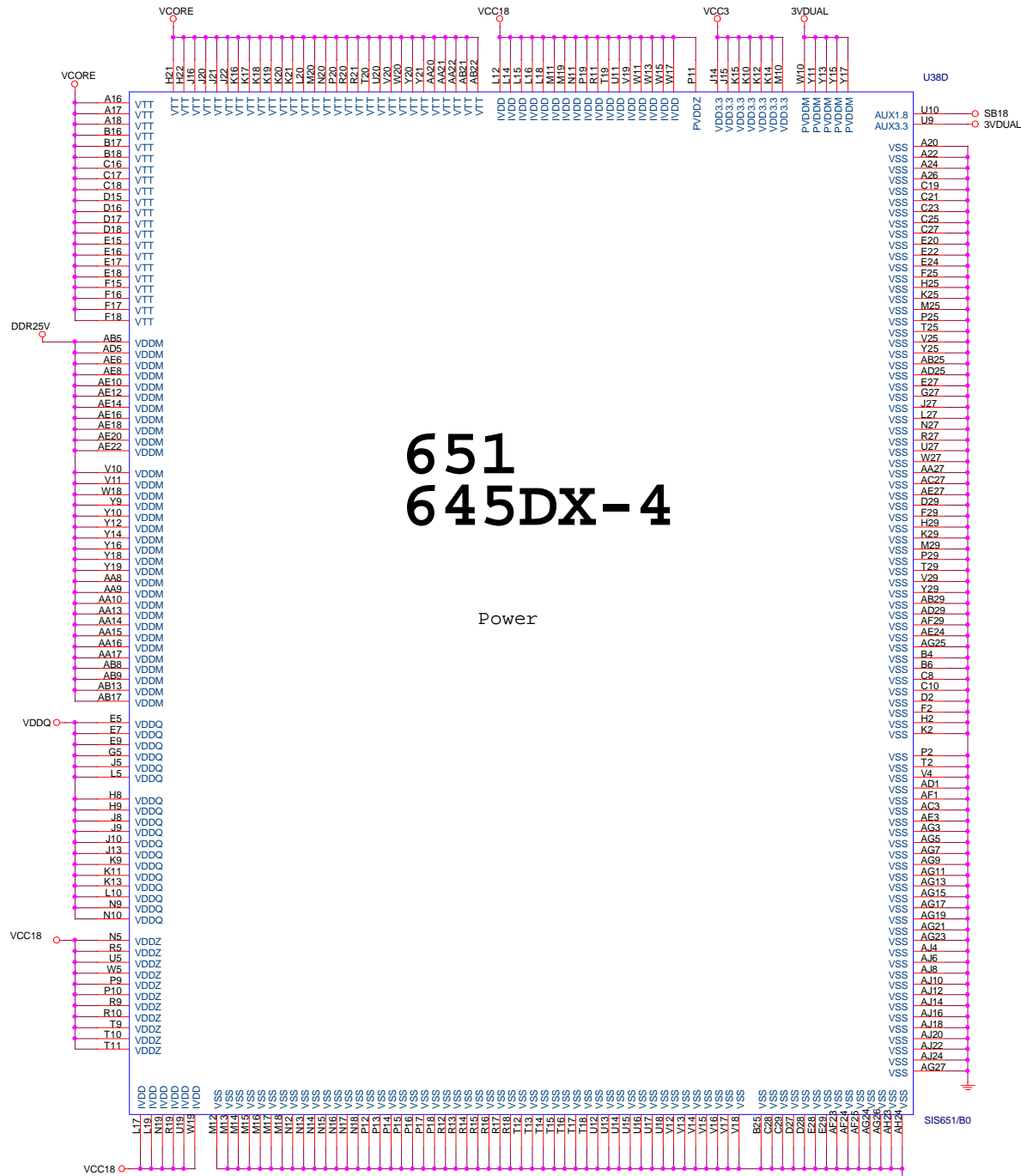


GIGABYTE

Title			SIS651/645DX(HYPER ZIP)		
Size	Document Number	Rev		1.0	
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Date:	Wednesday, May 07, 2003	Sheet	9	of	32

651 645DX-4

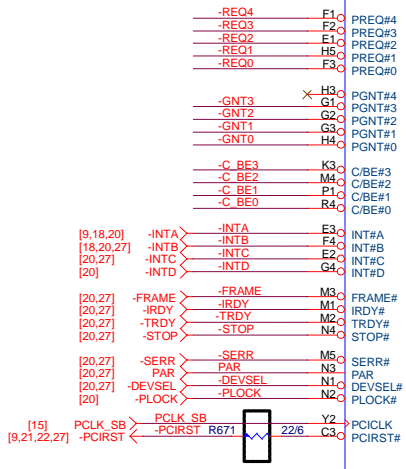
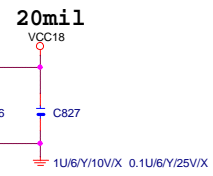
Power



GIGABYTE		
Title SIS651/645DX(PWR)		
Size Custom	Document Number GA-8S650GXM	Rev 1.0
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PDD0..15] <-> PDD[0..15] [21]
 SDD0..15] <-> SDD[0..15] [21]
 -REQ0..4] <-> -REQ[0..4] [20,27]
 -GNT0..3] <-> -GNT[0..3] [20,27]
 -C_BE0..3] <-> -C_BE[0..3] [20,27]
 AD0..31] <-> AD[0..31] [20,27]

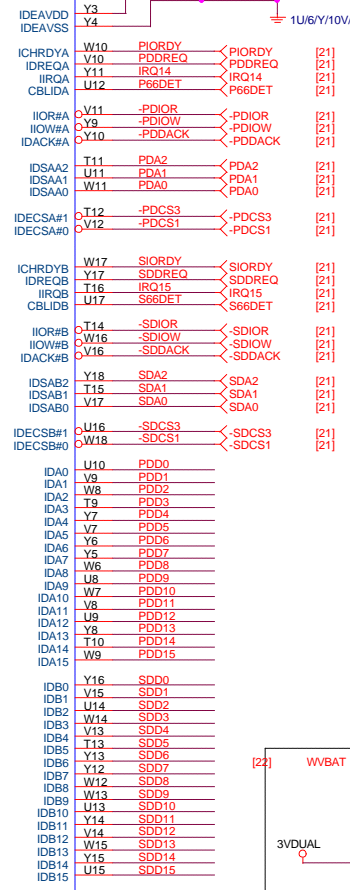
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0



PCI

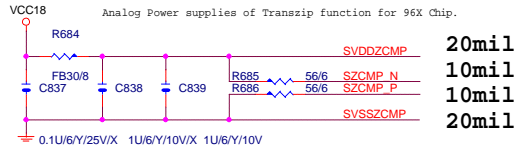
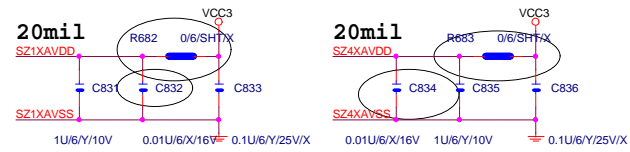
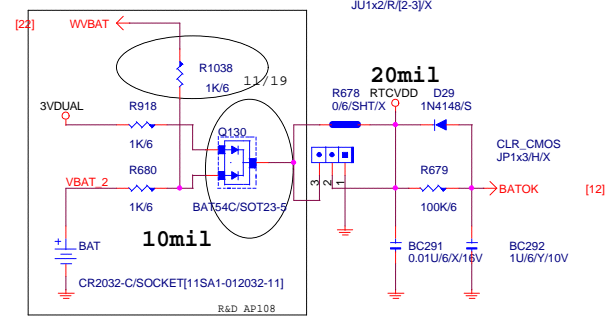
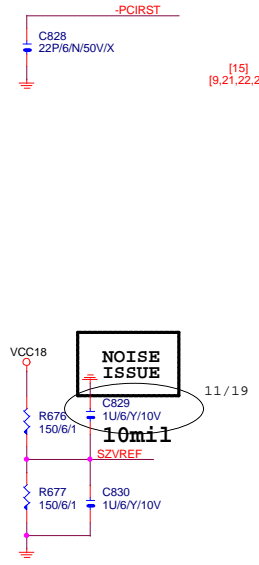
IDE

962/961B



HyperZip

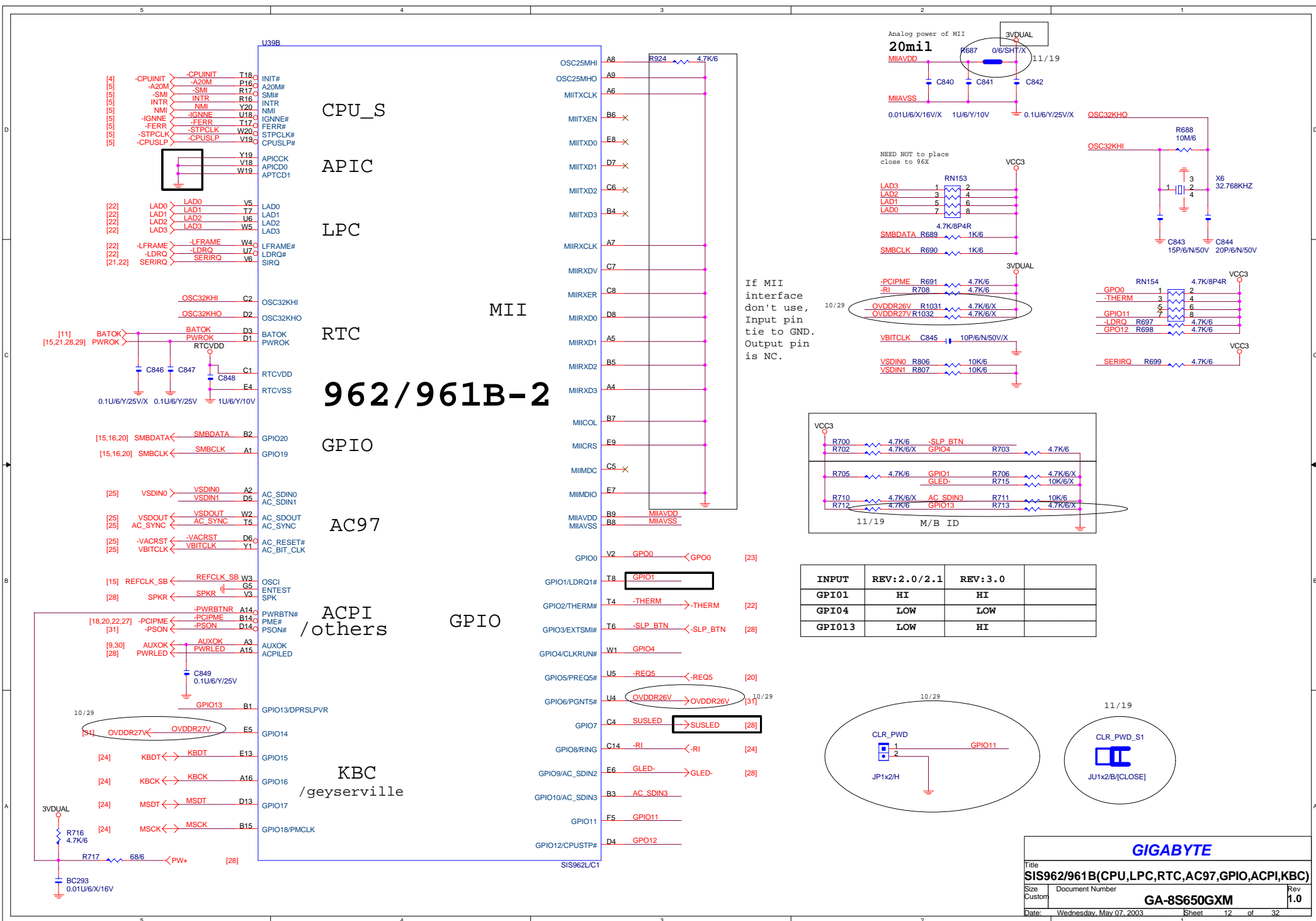
CLR_CMOS	CLEAR COMS JUMPER
1-2	Enable
2-3	Normal (Default)



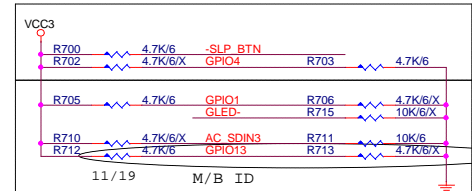
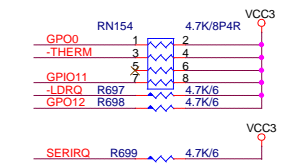
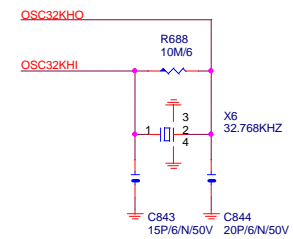
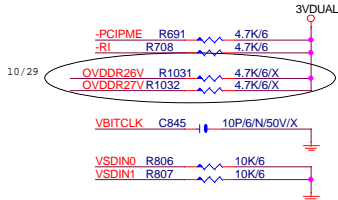
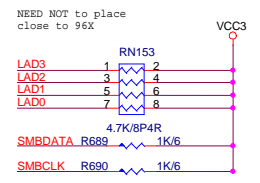
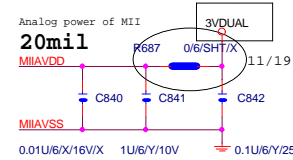
Analog Power supplies of Transzip function for 96X Chip.

NF REQUEST CLR_CMOS

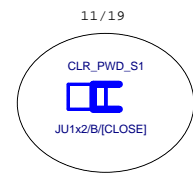
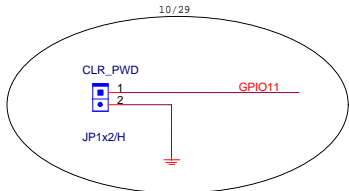
GIGABYTE		
Title SIS962(HP ZIP,PCI,IDE)		
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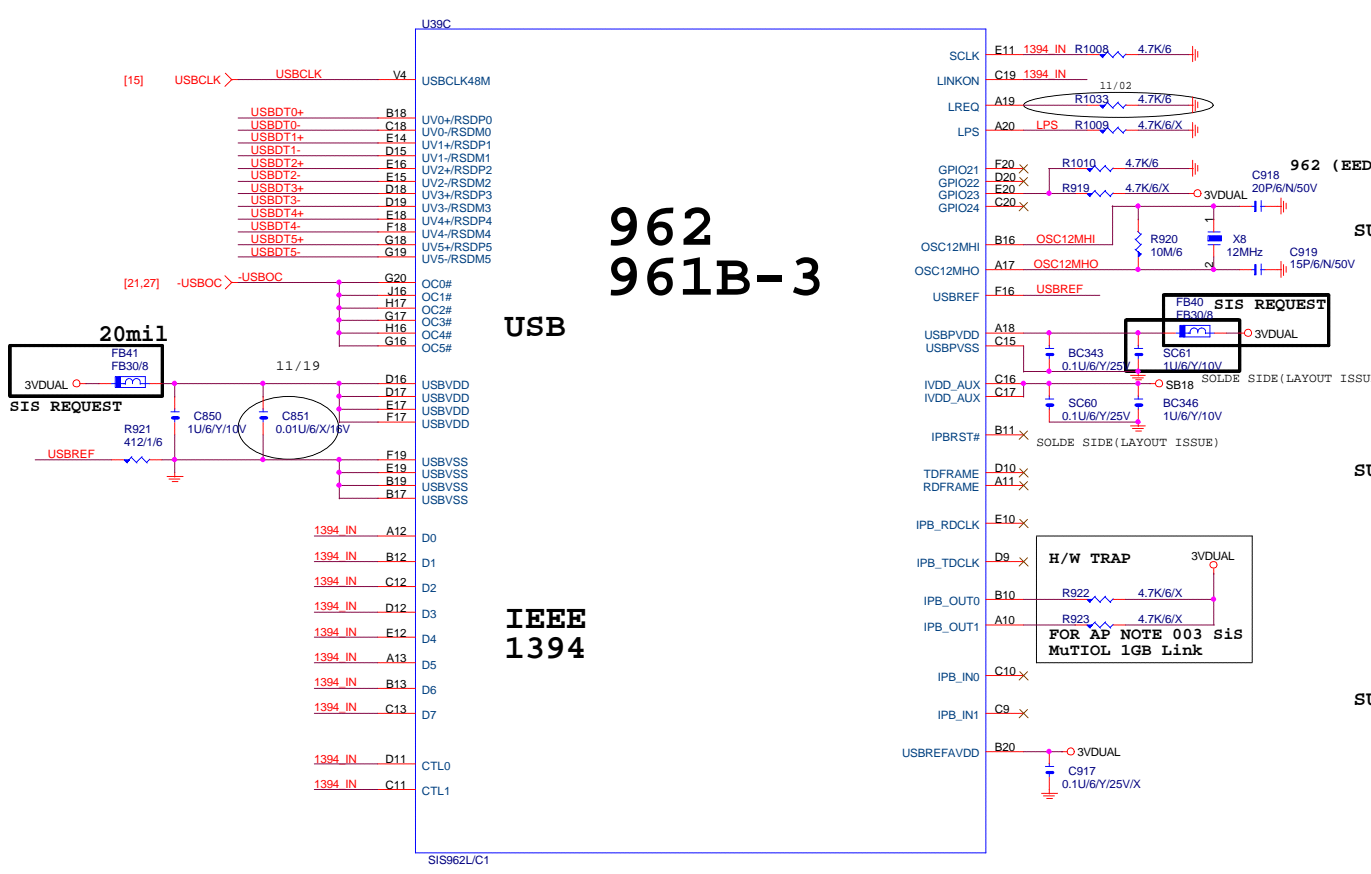
If MII interface don't use, Input pin tie to GND. Output pin is NC.



INPUT	REV: 2.0/2.1	REV: 3.0
GPIO1	HI	HI
GPIO4	LOW	LOW
GPIO13	LOW	HI



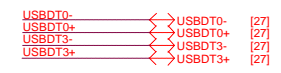
10/29



962 961B-3

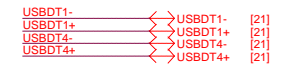
USB

IEEE 1394



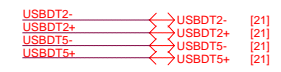
SUPPORT SIS962 ONLY POP 0/8P4R(USB2.0)

10/29



SUPPORT SIS962 ONLY POP 0/8P4R(USB2.0)

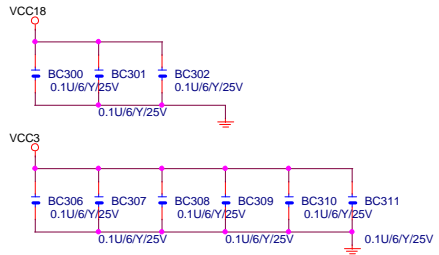
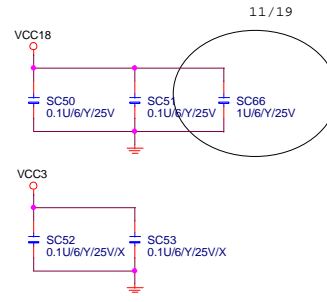
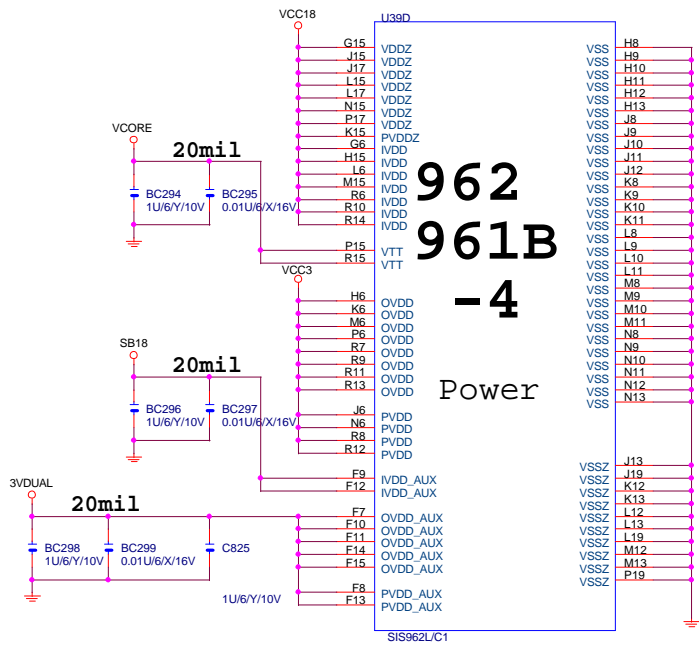
10/29



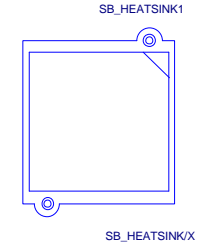
SUPPORT SIS962 ONLY POP 0/8P4R(USB2.0)

AGPUSB,CNRUSB DEFAULT NO POP
NOTE: POP CN3 15K/8P4R---->USB PULL DOWN
USB CONTROLLER MUST NOT BEEN FLOATING.

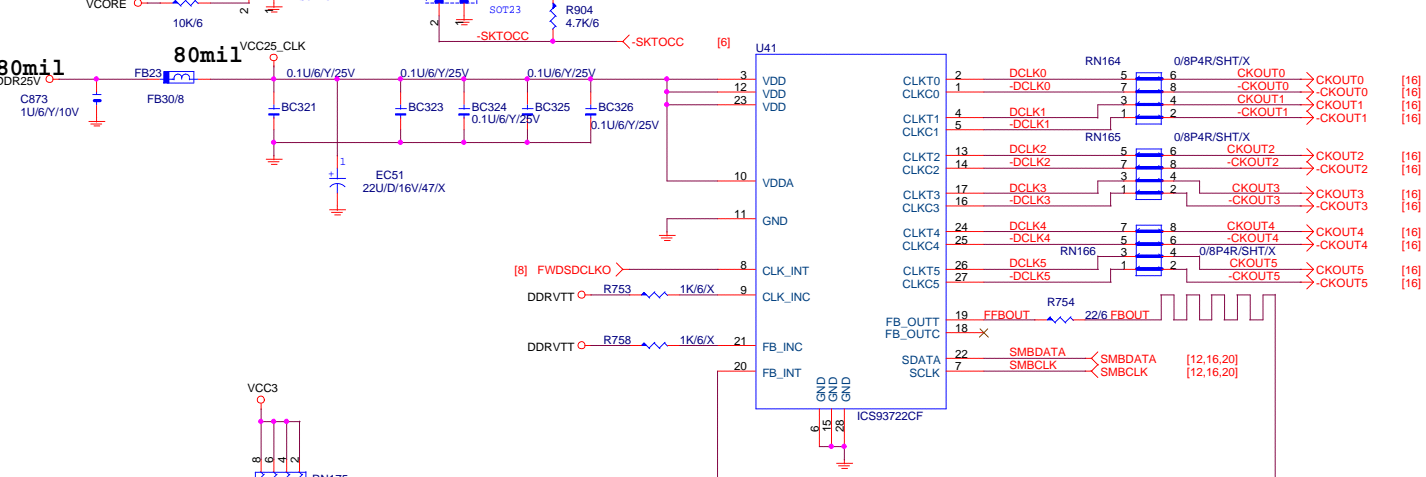
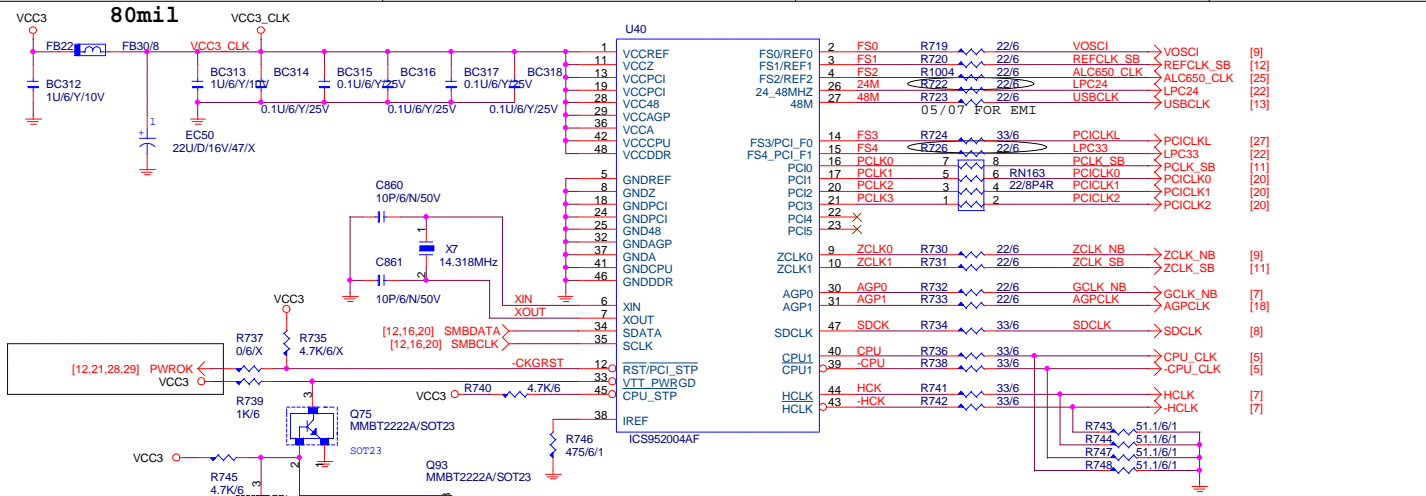
GIGABYTE		
Title SIS962/961B(USB20,1394)		
Size Custom	Document Number GA-8S650GXM	Rev 1.0
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S.B HEATSINK

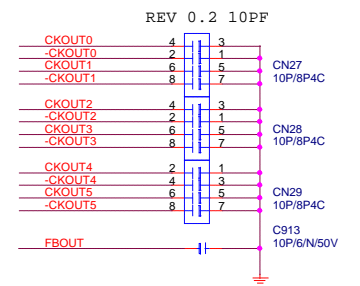
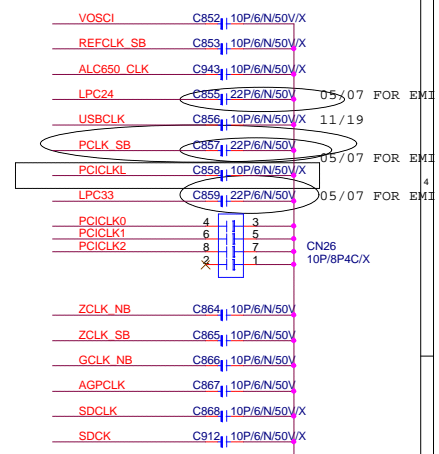
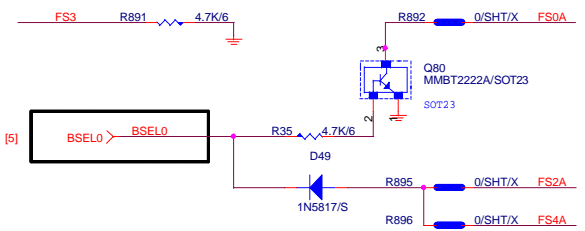


GIGABYTE		
Title		
SIS962/961B(PWR)		
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ICS952001/2004						
CPU	DDR	FS0	FS1	FS2	FS3	FS4
100	133	1	1	0	0	0
133	133	0	1	1	0	1

DEFAULT SETUP AUTO(100/133)



REV 0.2 10PF
DCLK +/----->0 ohm ADD CAP 10PF (clear glitch)

GIGABYTE

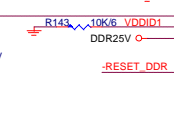
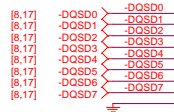
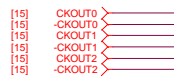
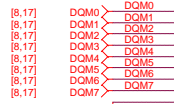
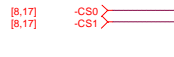
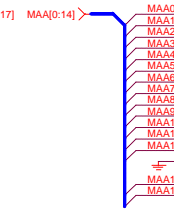
Title
CLOCK GEN + DDR BUFFER

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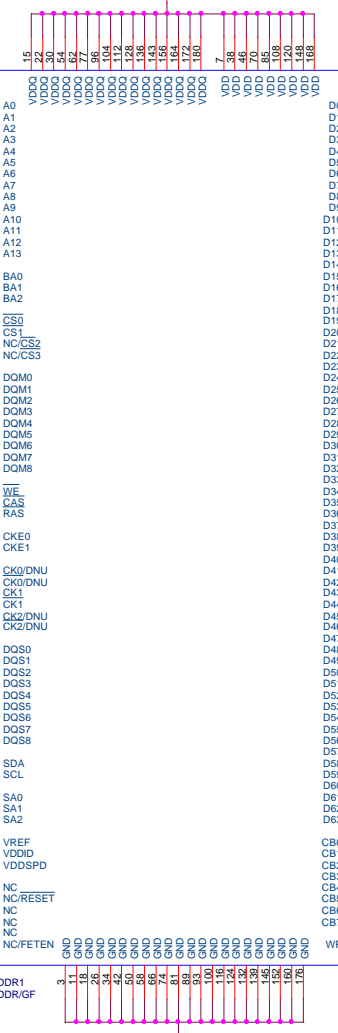
DDR SDRAM 1,2

SIS ONLY MAA

[8,17] MAA[0:14]

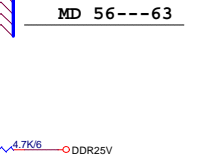
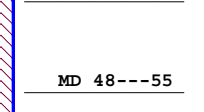
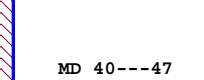
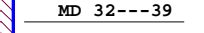
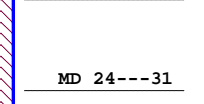
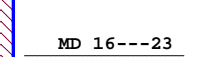
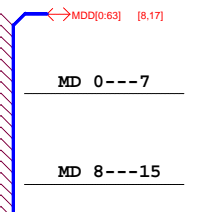


DDR25V

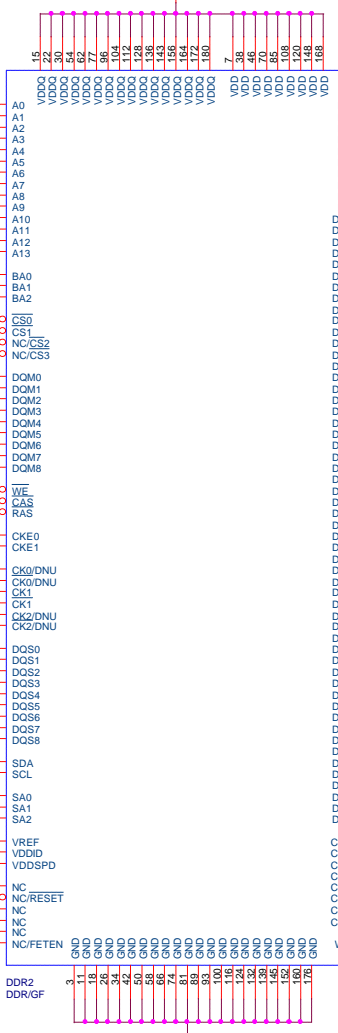


DDR MD GROUP SWAP

MDD[0:63] [8,17]

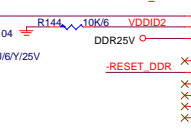
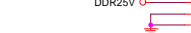
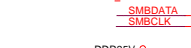
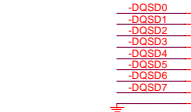
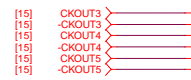
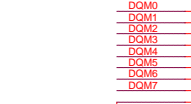
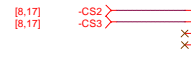
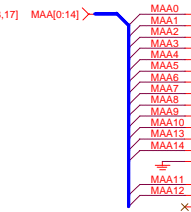


DDR25V



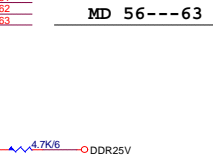
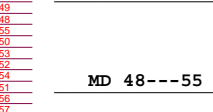
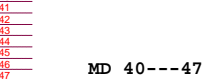
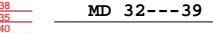
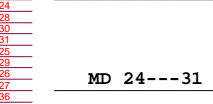
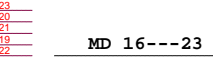
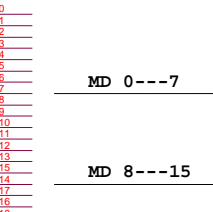
SIS ONLY MAA

[8,17] MAA[0:14]

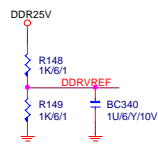


DDR MD GROUP SWAP

MDD[0:63] [8,17]

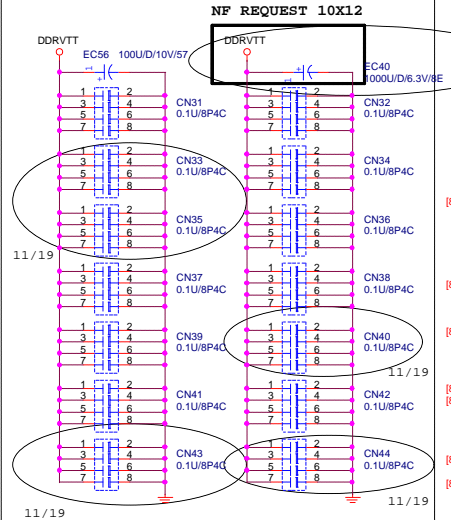


For Register DDR Support



GIGABYTE		
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DDRVTT Decouple

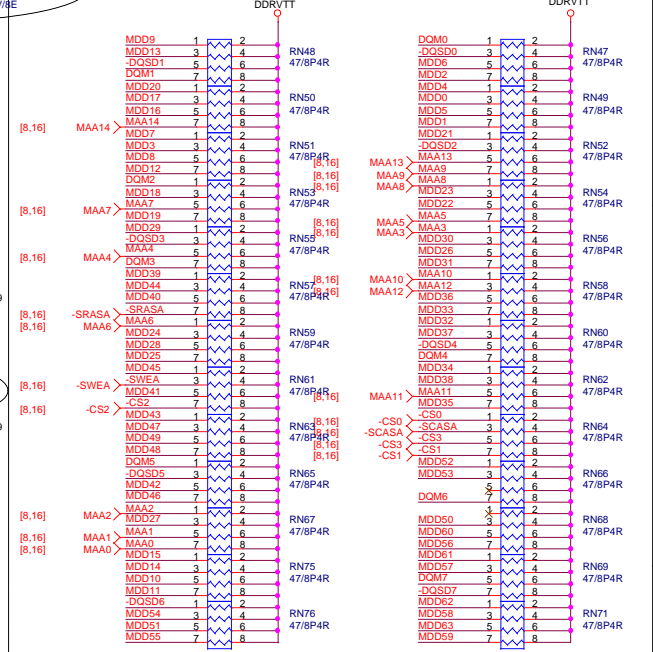


R&D NOTE 109 (0.1U/8P4C X9PCS)

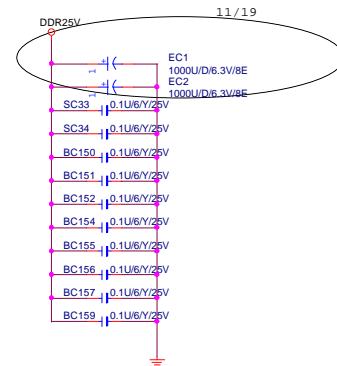
NOTE: Place these decoupling capacitors close to VTT_MEM termination resistors. (one decoupling capacitor for each two R-packs)

DDR TERMINATION

REV 0.2 DDR DIMM ISSUE
33-->47 OHM

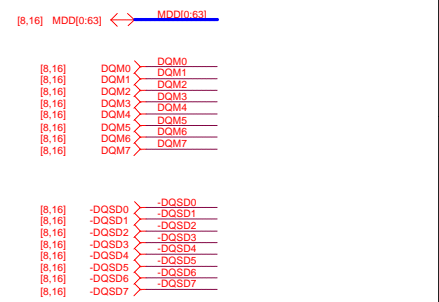
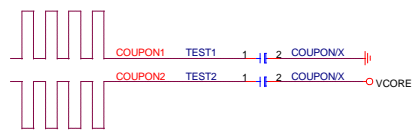


DDR25V Decouple

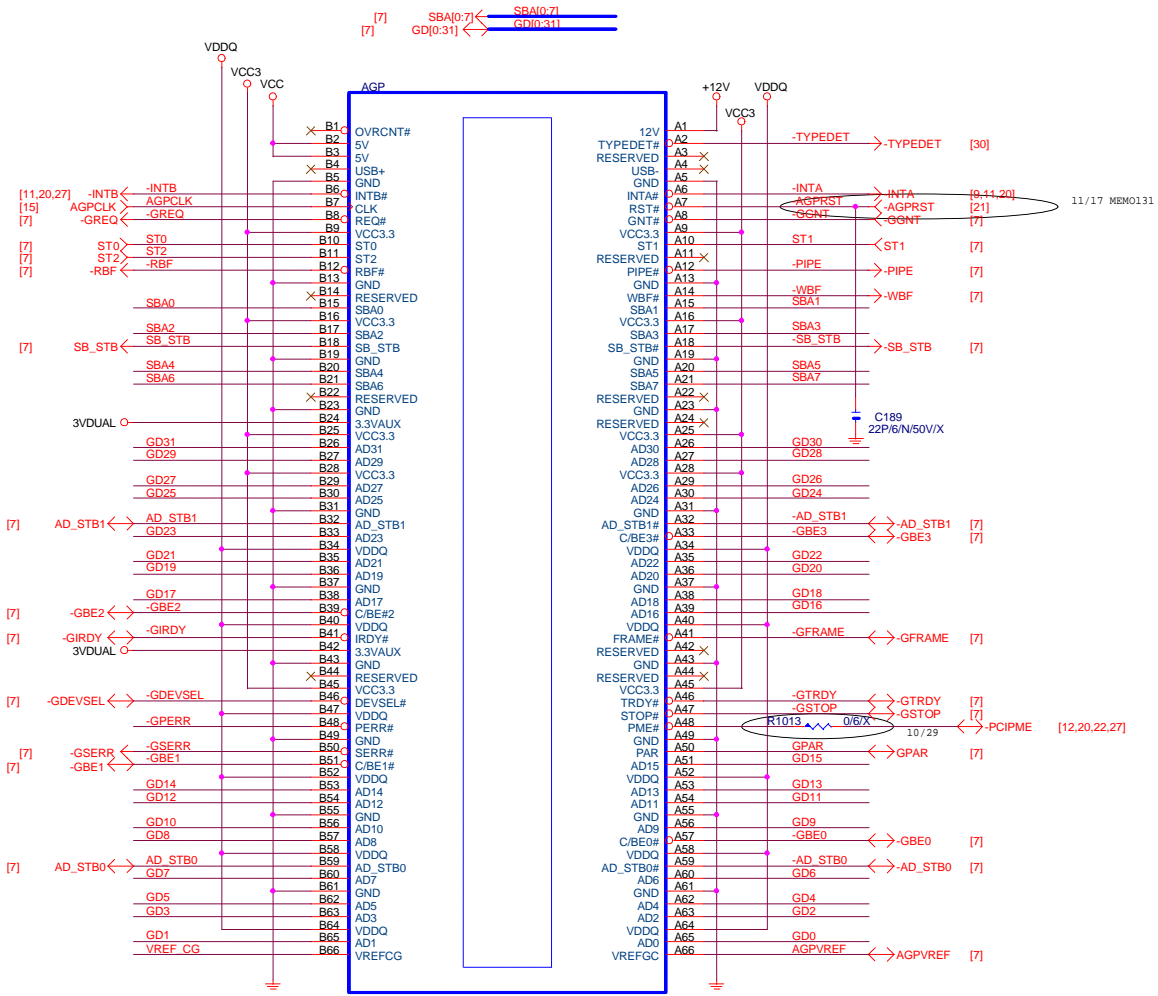


NOTE: Place Dretribute 4 pcs per DDR module.

IMPEDENCE TESTING COUPON

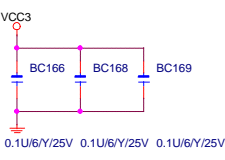


GIGABYTE			
DDR UNBUFFERED 3			
Size	Document Number	Rev	
Custom	GA-8S650GXM	1.0	
Date:	Wednesday, May 07, 2003	Sheet	17 of 32



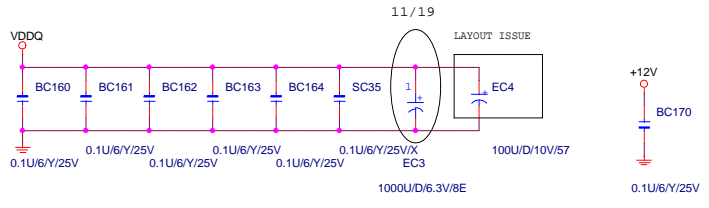
UAGP132/CO/GF
REV 0.2 AGP BOM MODIFY
11AC1-05R124-11

AGP SLOT (AGP-N)



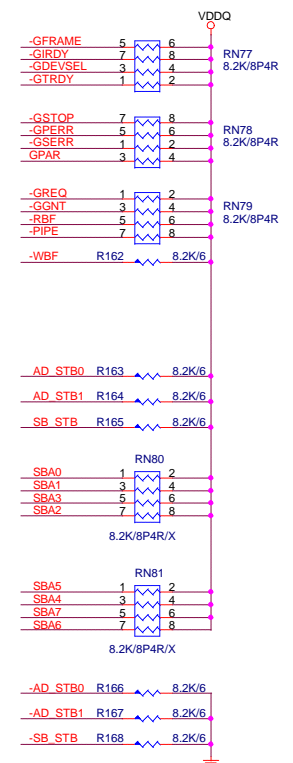
Place 1 at each pair of 3.3V pins

Decoupling capacitors
(Place near AGP slot)

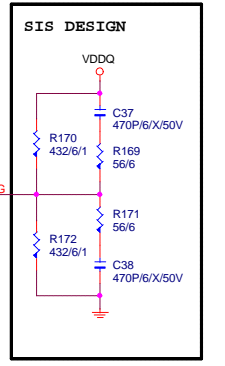
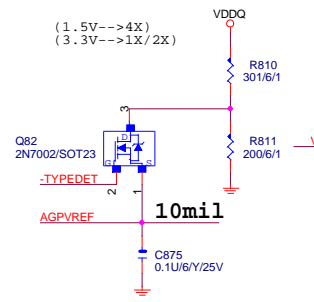


Place 1 at each pair of VDDQ pins

Place an additional for spread from A14 - A33



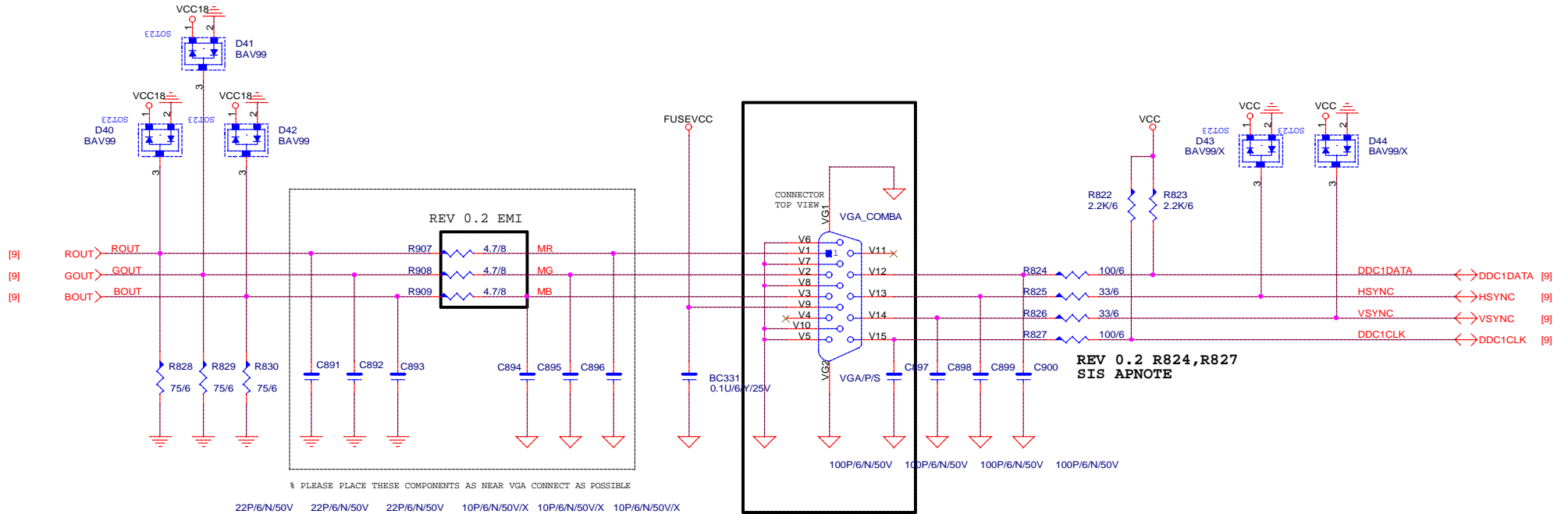
SWITCH CIRCUIT FOR VDDQ



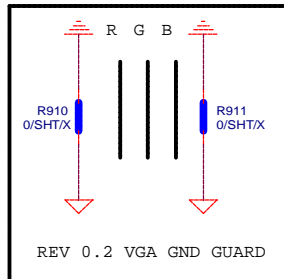
GIGABYTE		
AGP SLOT		
Title	AGP SLOT	
Size	Document Number	Rev
Custom	GA-8S650GXM	1.0
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VGA CONNECTOR 1

SIS 645DX NO POP



DUAL LAYOUT (VGA/COM)



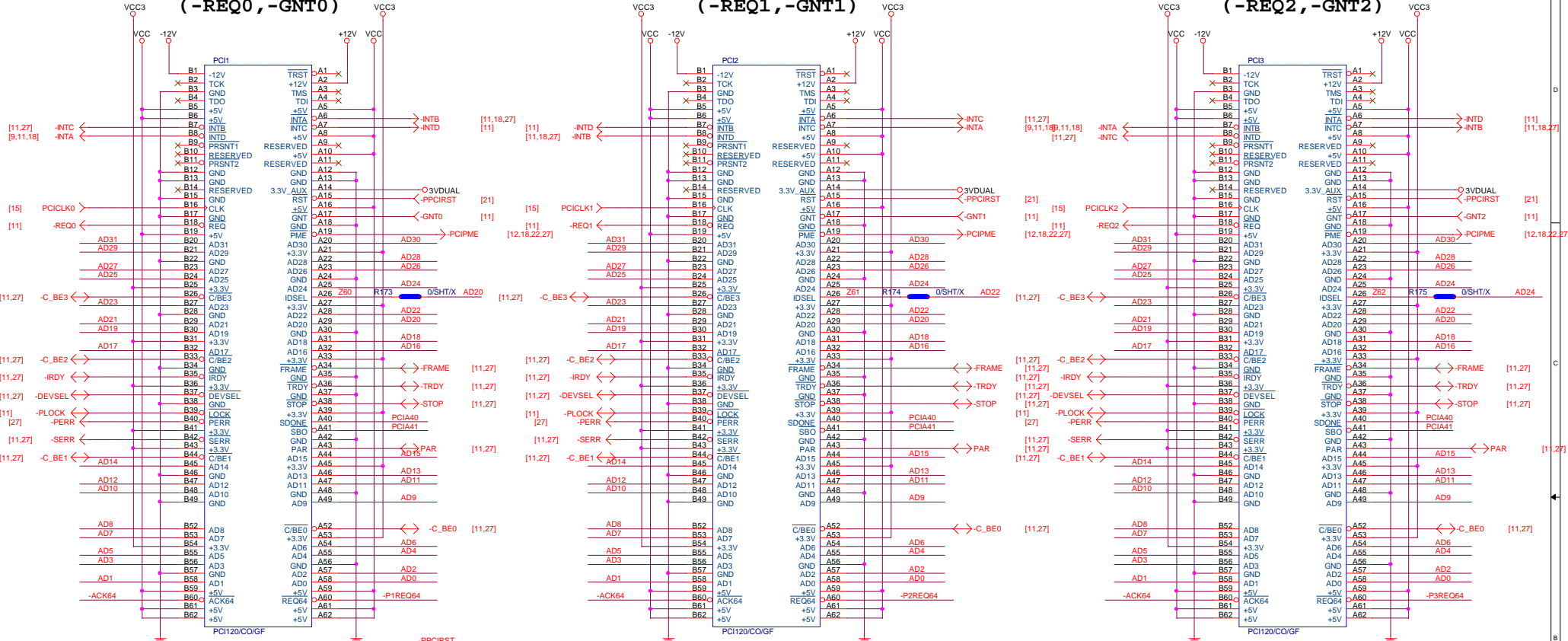
GIGABYTE		
Title VGA CONNECTOR		
Size B	Document Number GA-8S650GXM	Rev 1.0
Date: Wednesday, May 07, 2003	Sheet 19	of 32

PCI SLOT 1,2,3

PCI SLOT1 (-REQ0, -GNT0)

PCI SLOT2 (-REQ1, -GNT1)

PCI SLOT3 (-REQ2, -GNT2)



SIS-IDSEL(A20) (B)

SIS-IDSEL(A22) (C)

SIS-IDSEL(A24) (D)

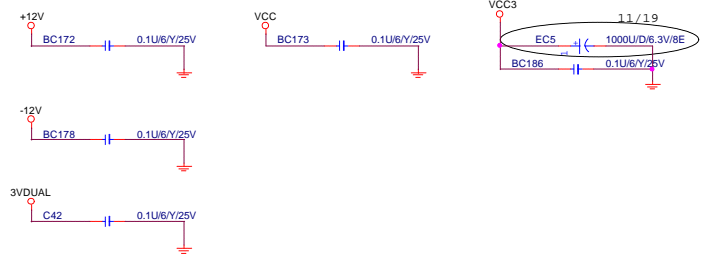
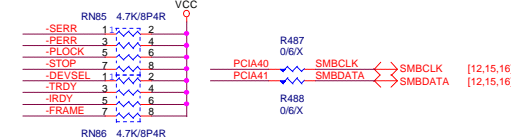
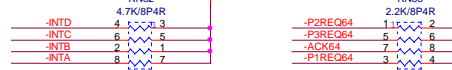
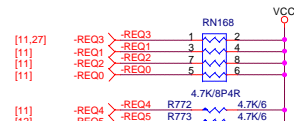
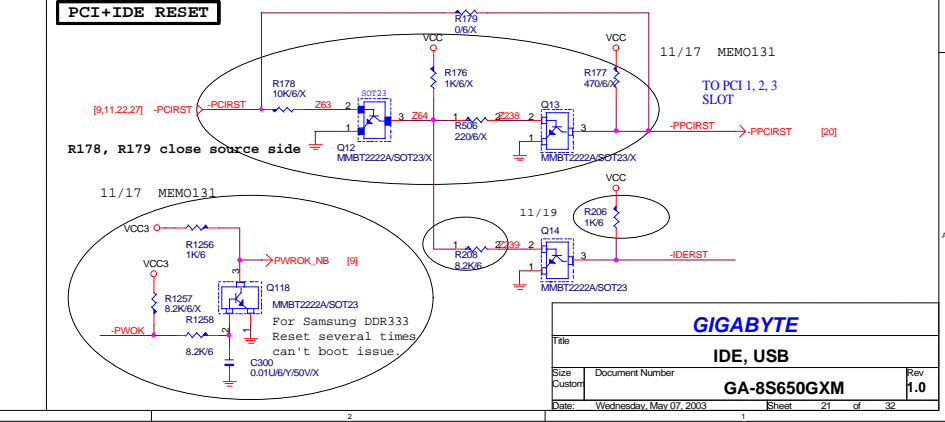
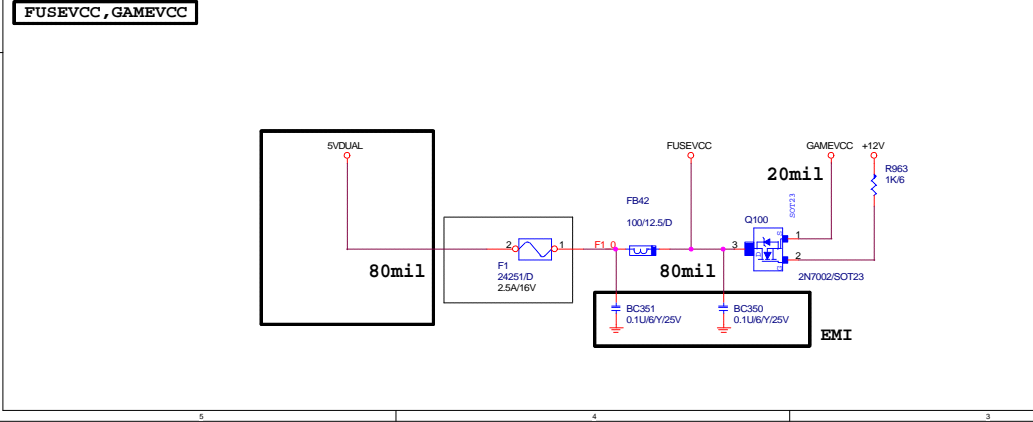
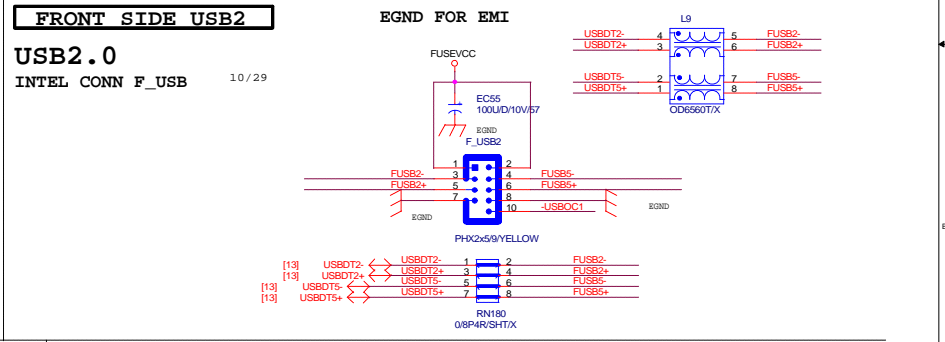
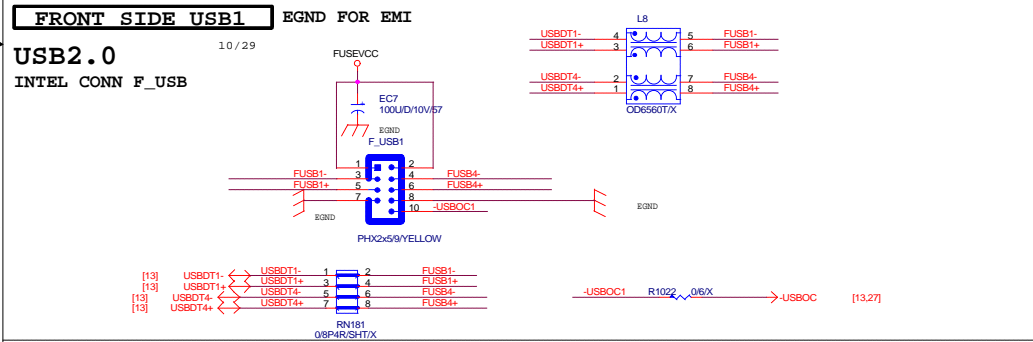
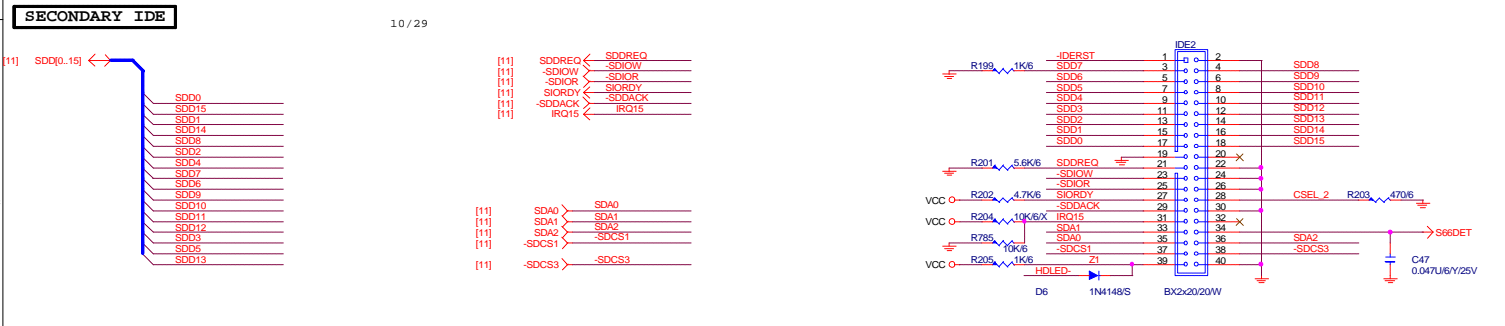
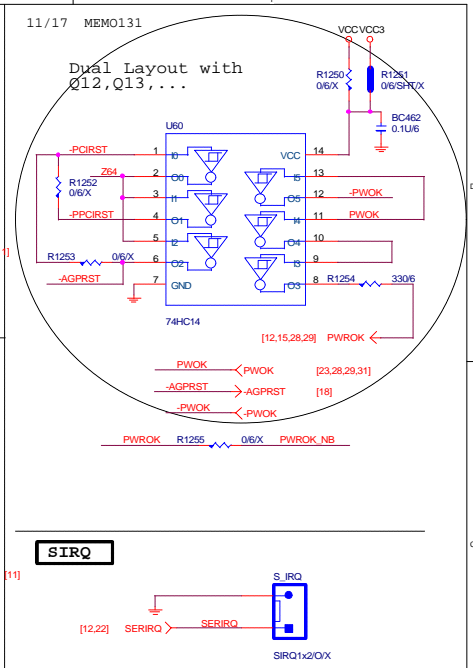
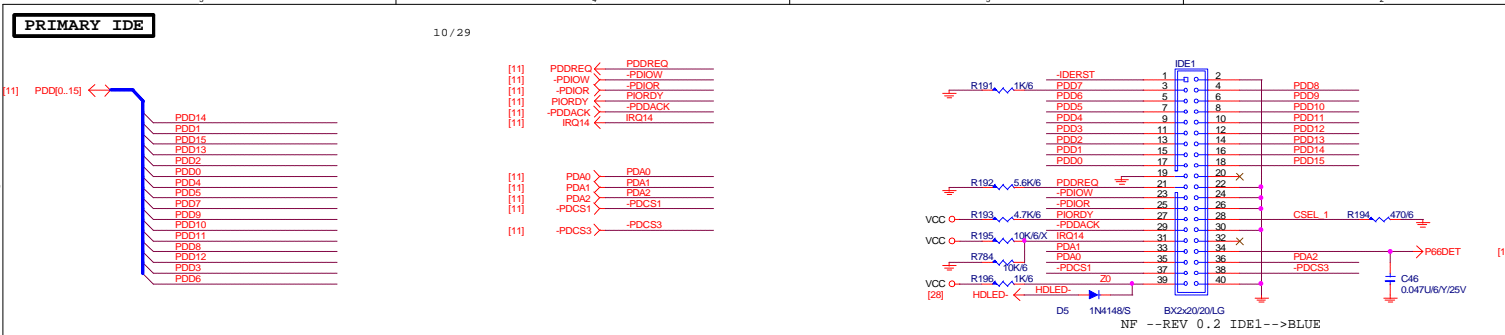
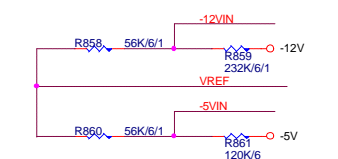
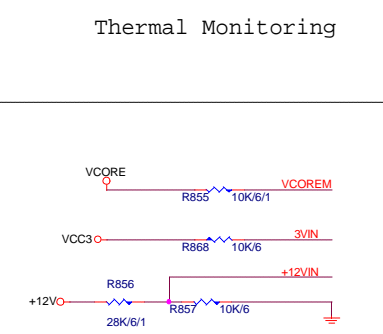
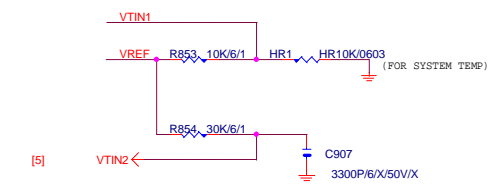
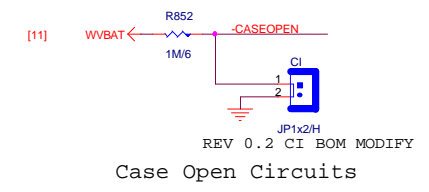
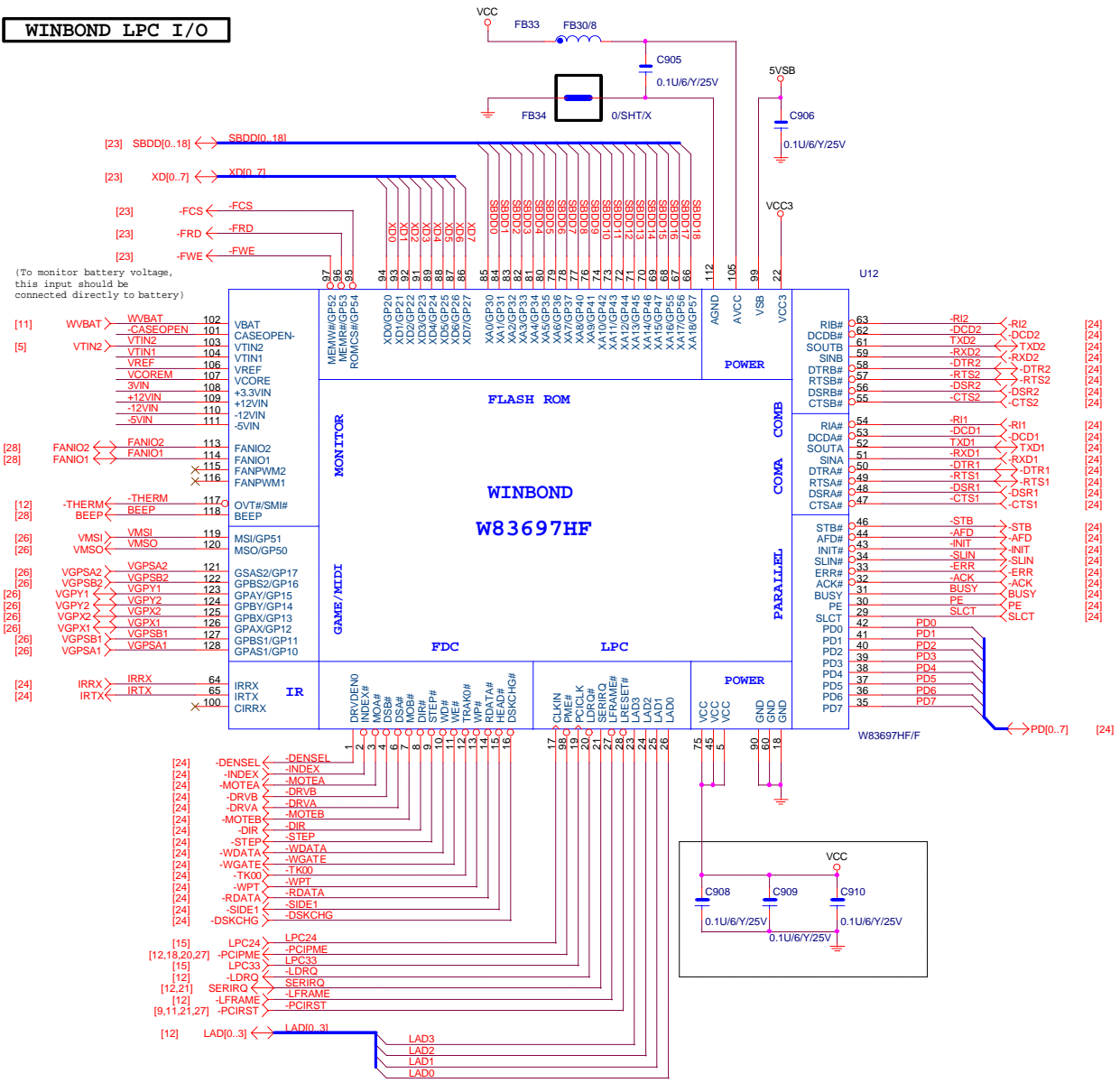


Table with GIGABYTE logo and product information: PCI SLOT 1,2,3, GA-8S650GXM, Rev 1.0, Date: Wednesday, May 07, 2003, Sheet 20 of 32.



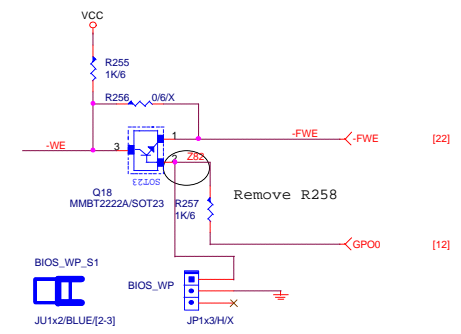
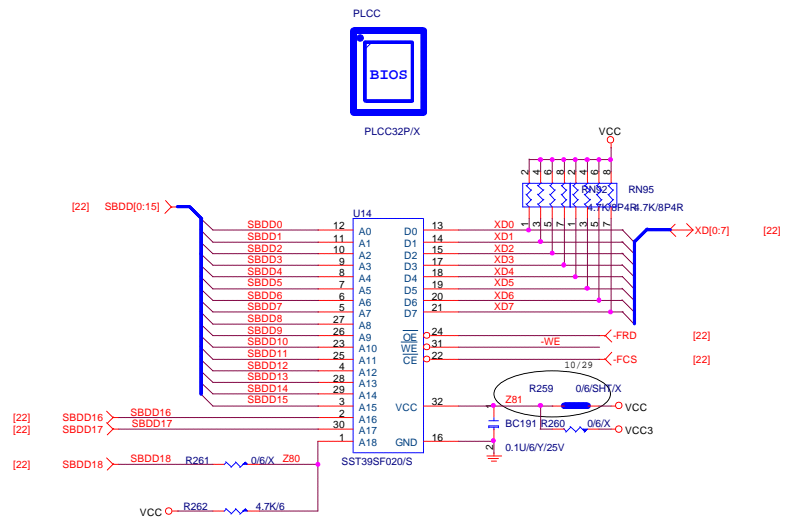
GIGABYTE		
Title: IDE, USB		
Size: Custom	Document Number: GA-8S650GXM	Rev: 1.0
Date: Wednesday, May 07, 2003	Sheet: 21	of 32

WINBOND LPC I/O



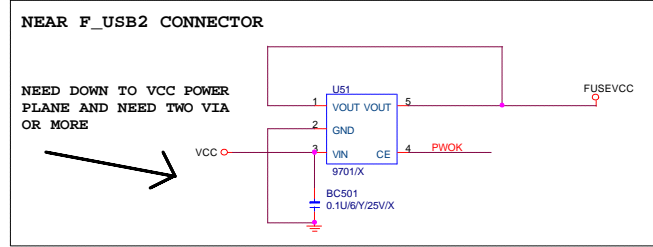
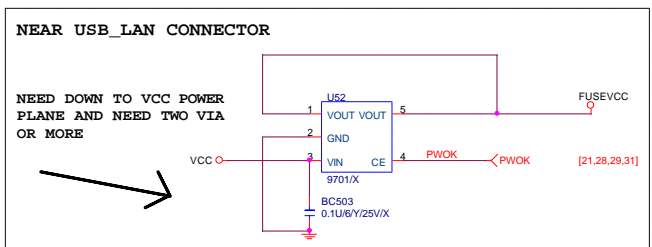
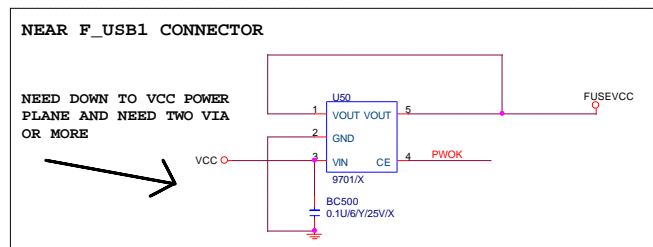
Voltage Monitoring

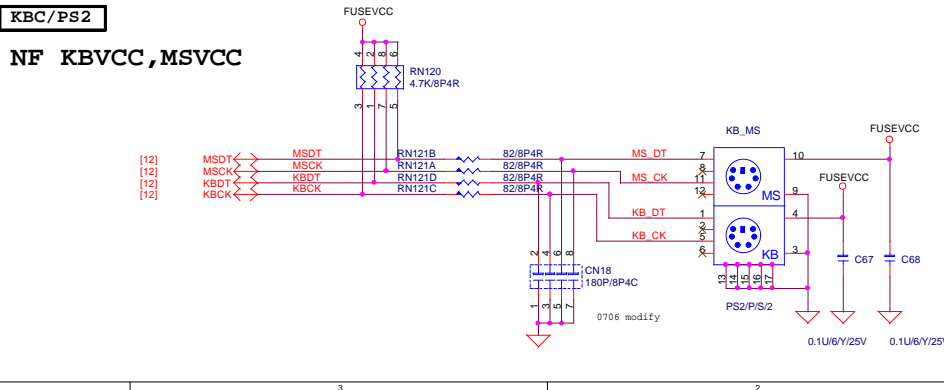
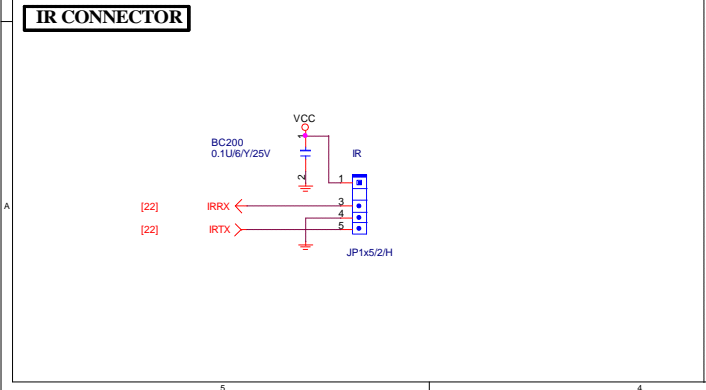
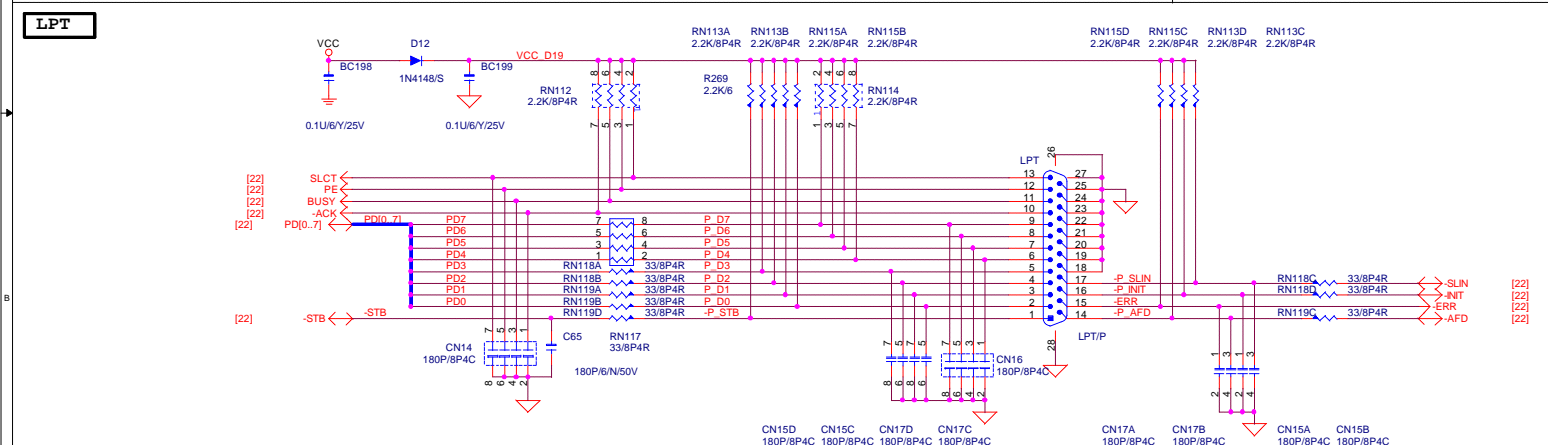
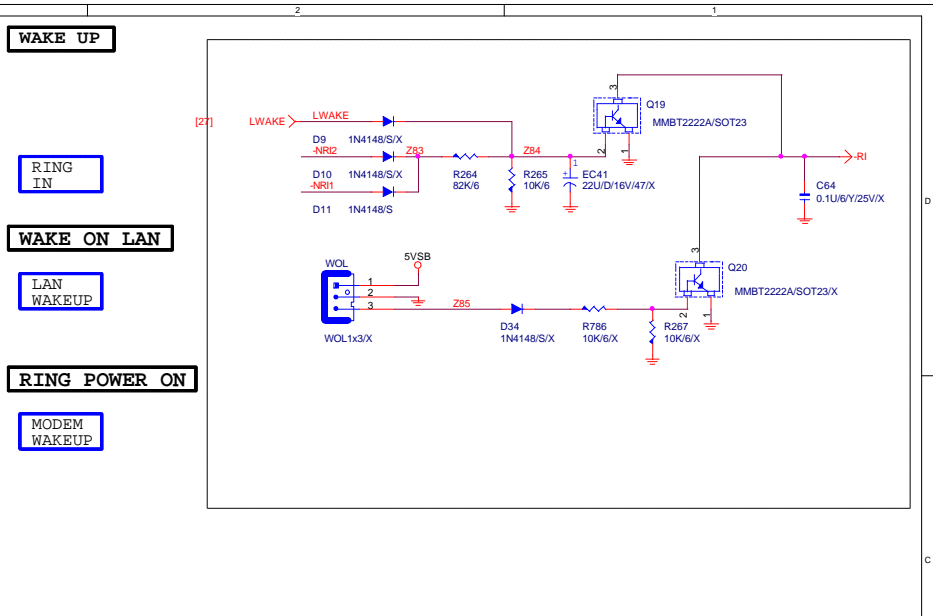
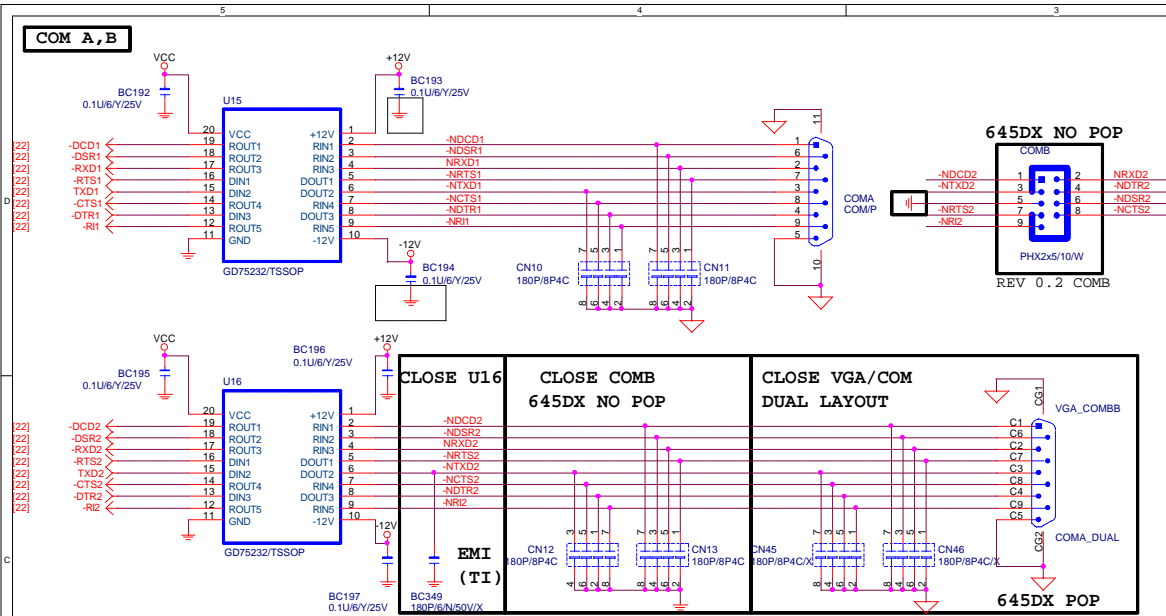
GIGABYTE		
LPC W83697		
Title		
Size	Document Number	Rev
Custom	GA-8S650GXM	1.0
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BIOS_WP: BIOS WRITE PROTECT

PIN	BIOS_WP
1-2	WRITE PROTECT
2-3	WRITE ENABLE (default)





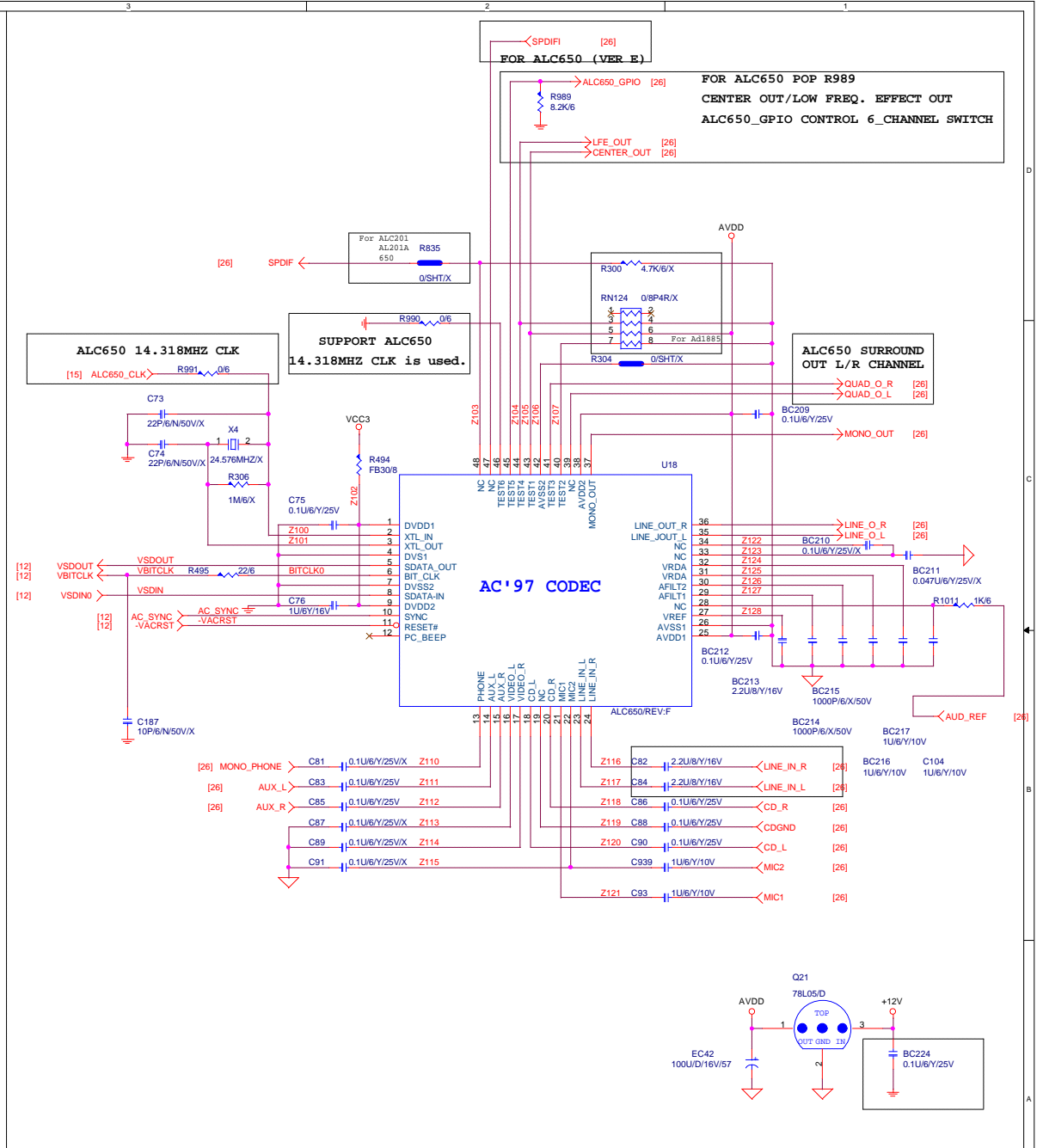
GIGABYTE			
COM,PRT,FDD,KB,IR			
Title	Document Number		
Size Custom	GA-8S650XGM		Rev 1.0
Date	Wednesday, May 07, 2003	Sheet 24	of 32

D

C

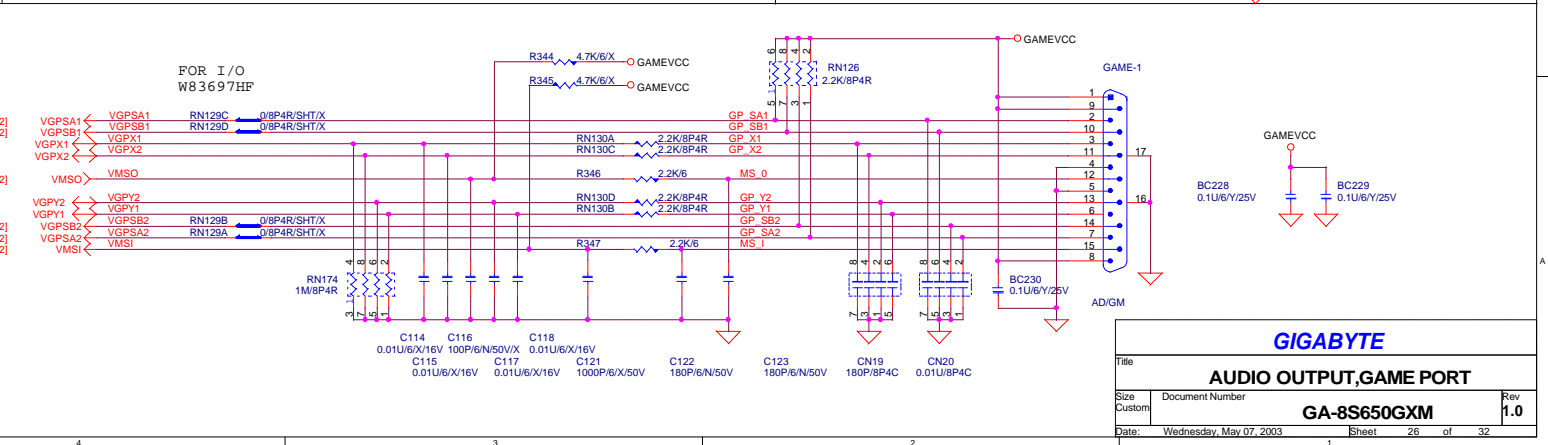
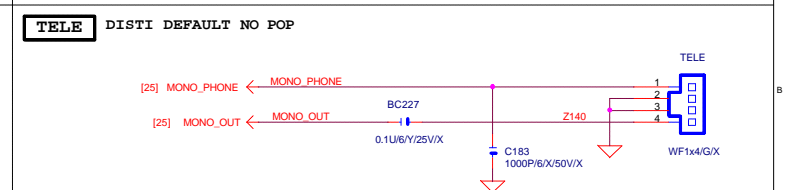
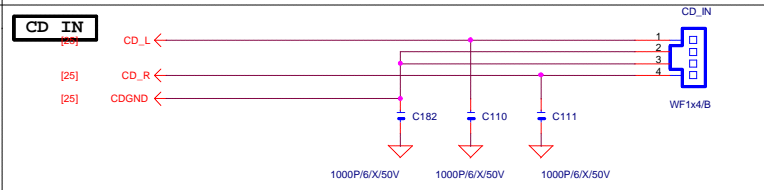
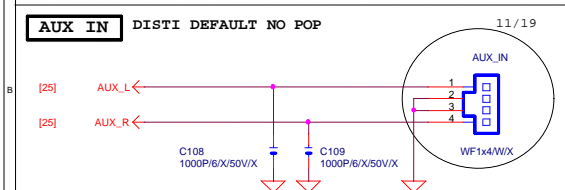
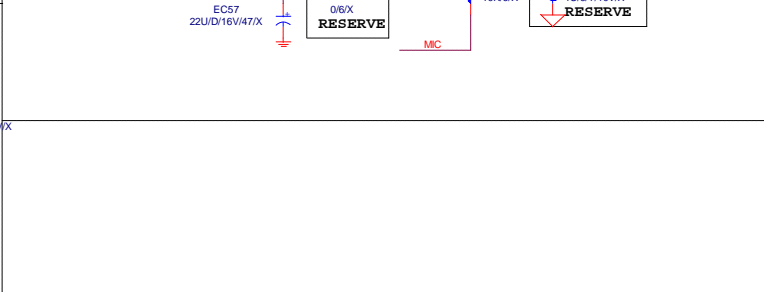
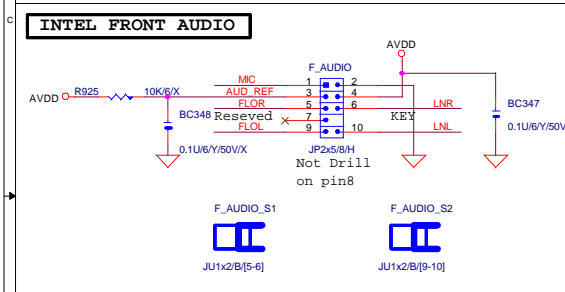
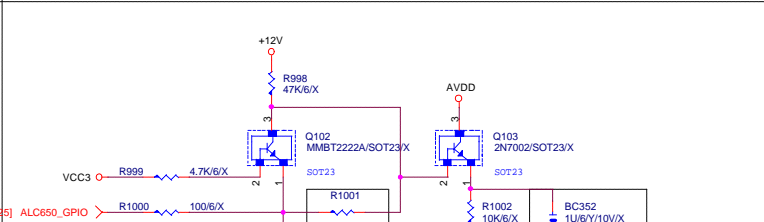
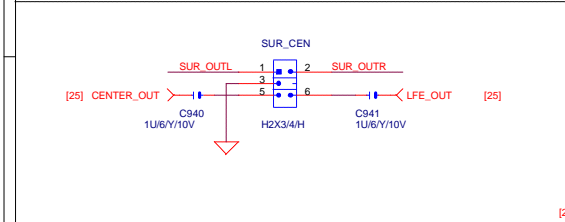
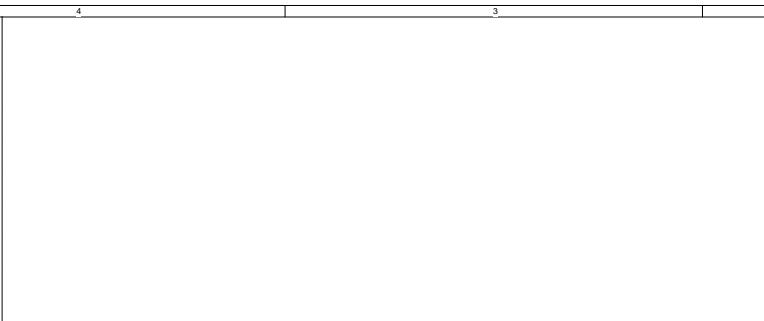
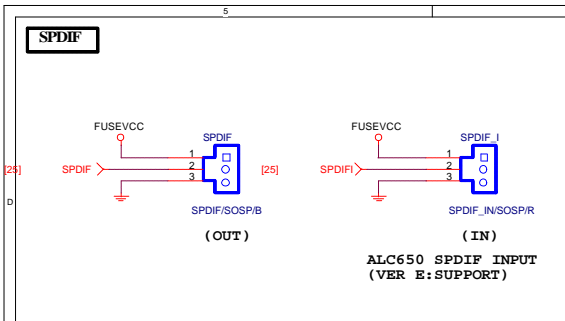
B

A

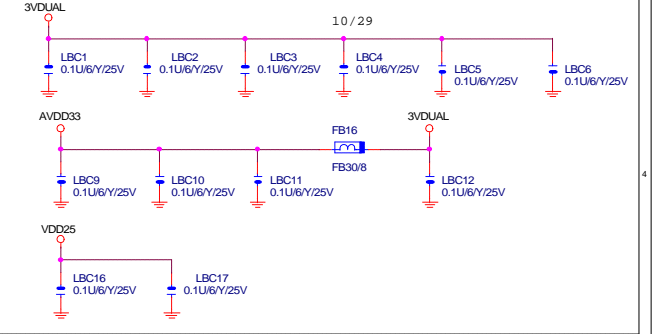
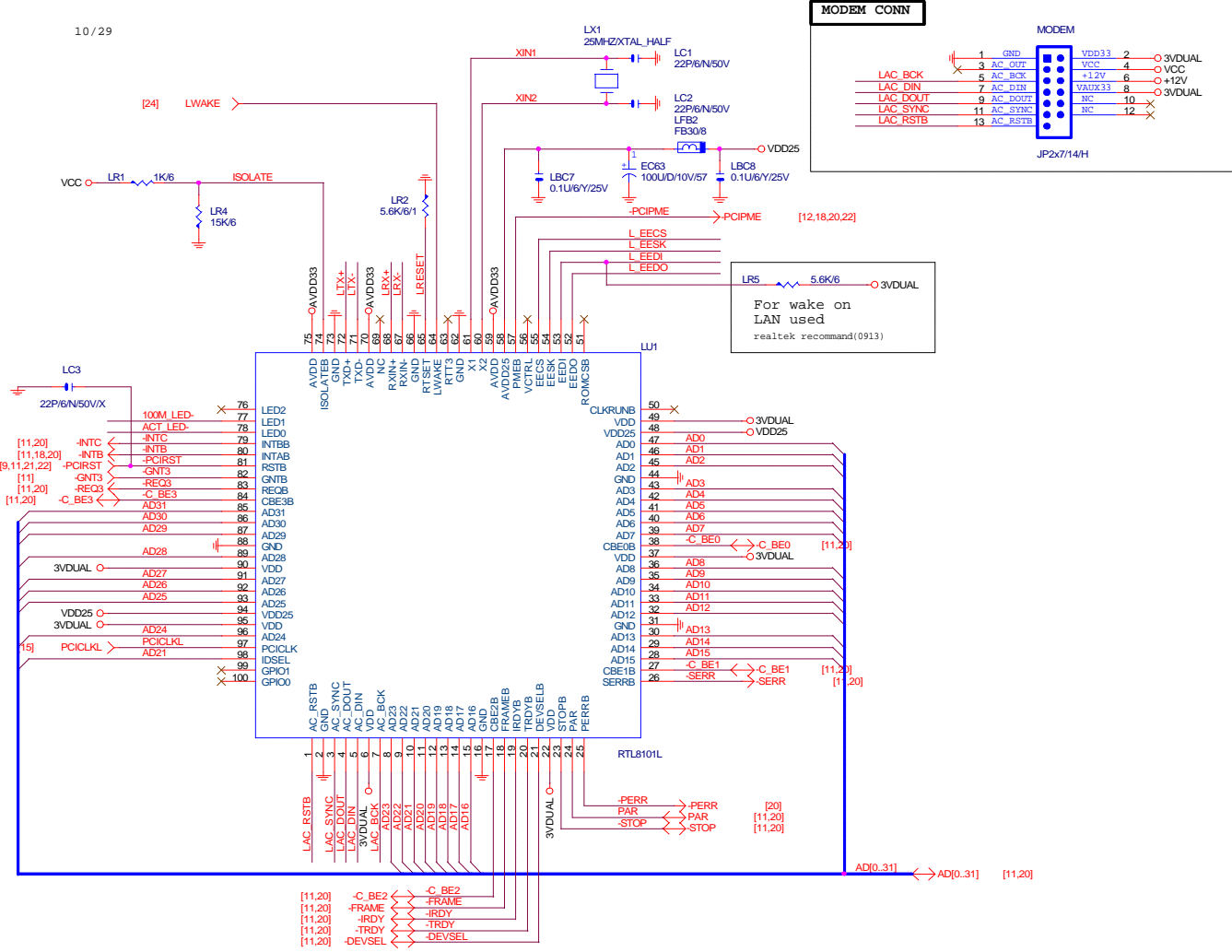


NF	SIGMATEL9756
Disti	ALC201A

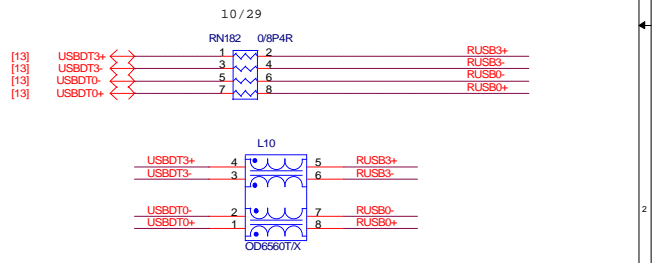
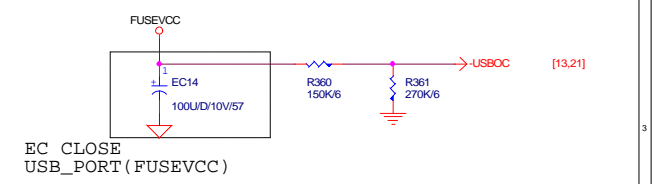
GIGABYTE			
AUDIO (AC97 CODEC)			
Title	Document Number	Rev	
	GA-8S650GX	1.0	
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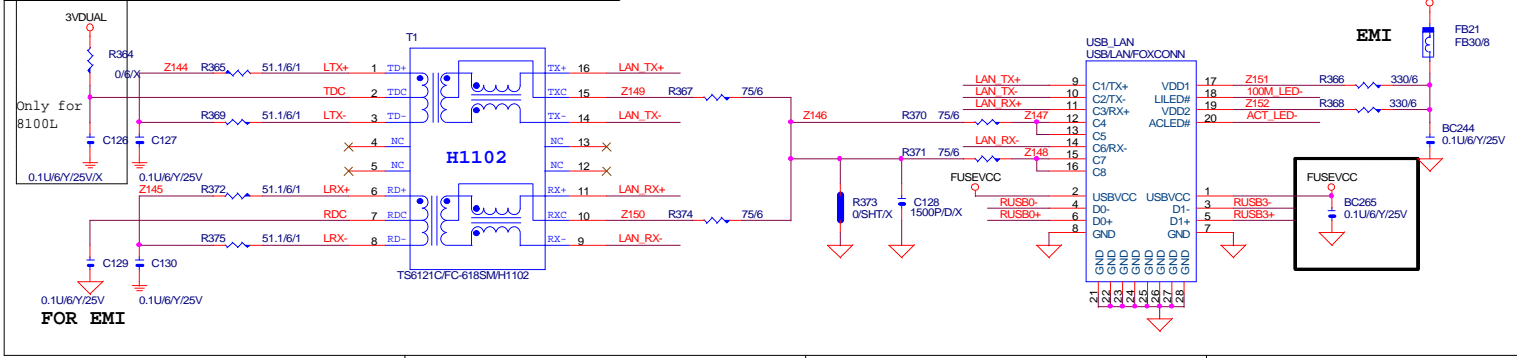
GIGABYTE	
Title	
AUDIO OUTPUT, GAME PORT	
Size	Document Number
Custom	GA-8S650GXM
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Rev	1.0



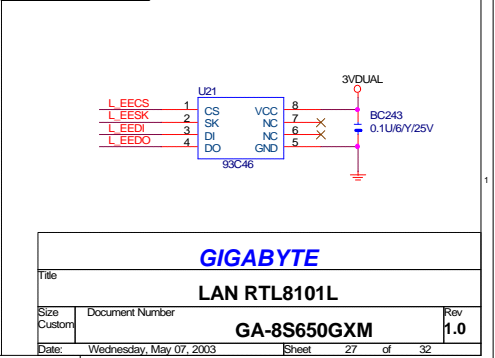
USB2.0 REAR USBX2



10/100M BASE TRANSFORMER (1:1)+FOXCONN (RJ45+USBX2)

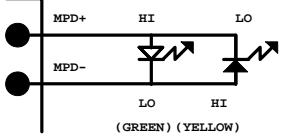


LAN EEPROM

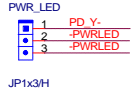


GIGABYTE		
LAN RTL8101L		
Title	Document Number	Rev
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FRONT PANEL



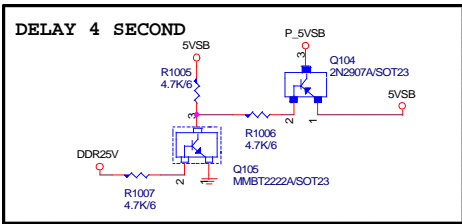
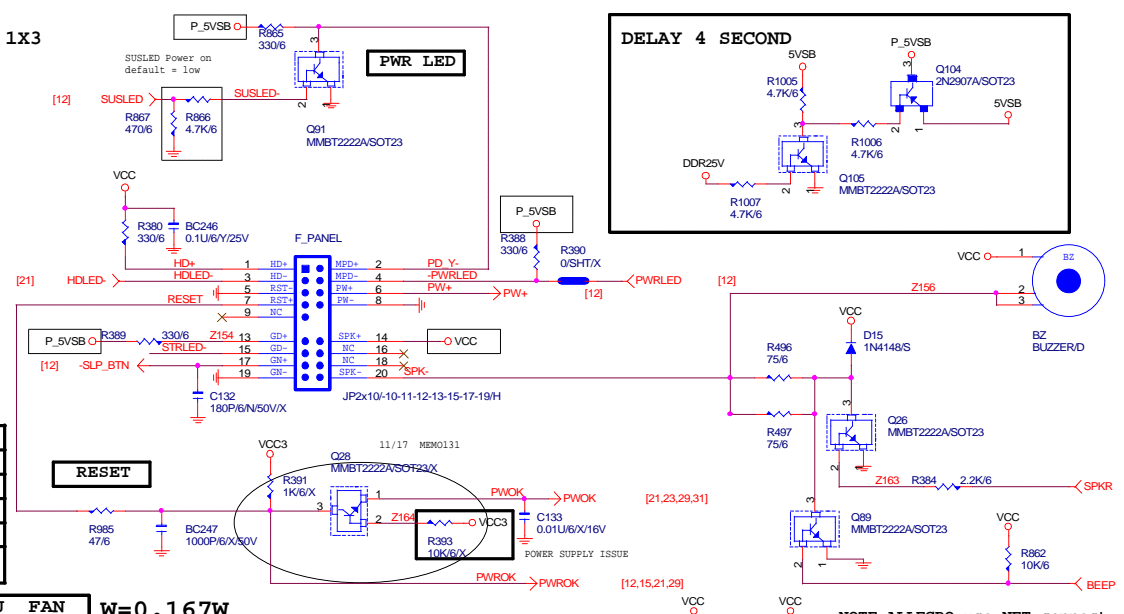
**PWR_LED FOR DISTI PIN 1X3
LED USED**



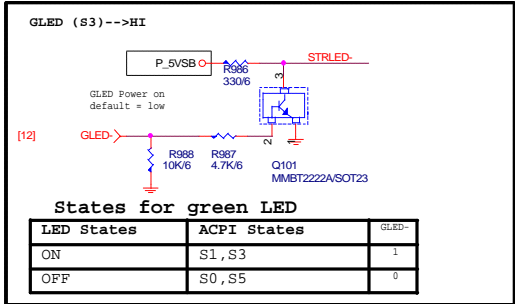
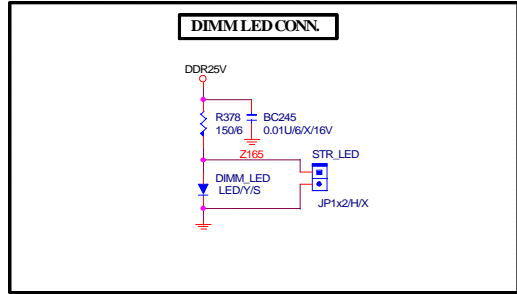
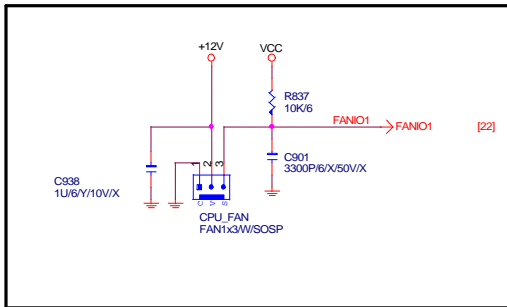
LED States	ACPI States	MPD+	MPD-
OFF	S1,S3,S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING

States for a dual-color power LED

LED States	ACPI States	MPD+	MPD-
OFF	S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING
Steady Yellow	S1,S3	LO	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING



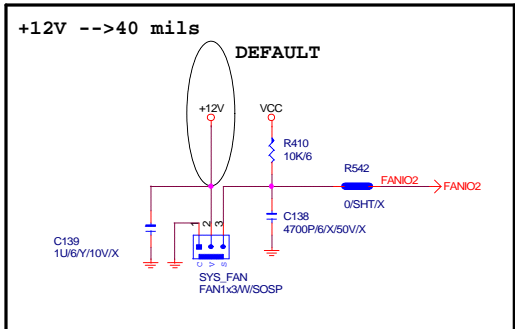
CPU FAN W=0.167W



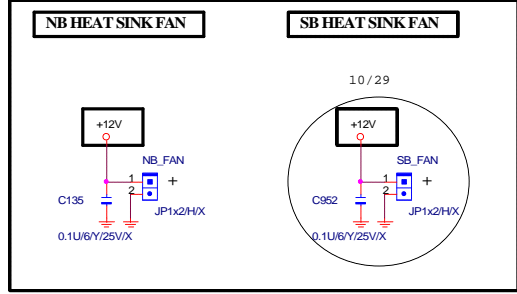
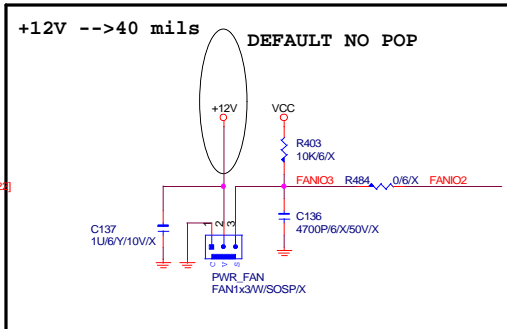
States for green LED

LED States	ACPI States	GLED-
ON	S1,S3	1
OFF	S0,S5	0

SYSTEM FAN W=0.167W



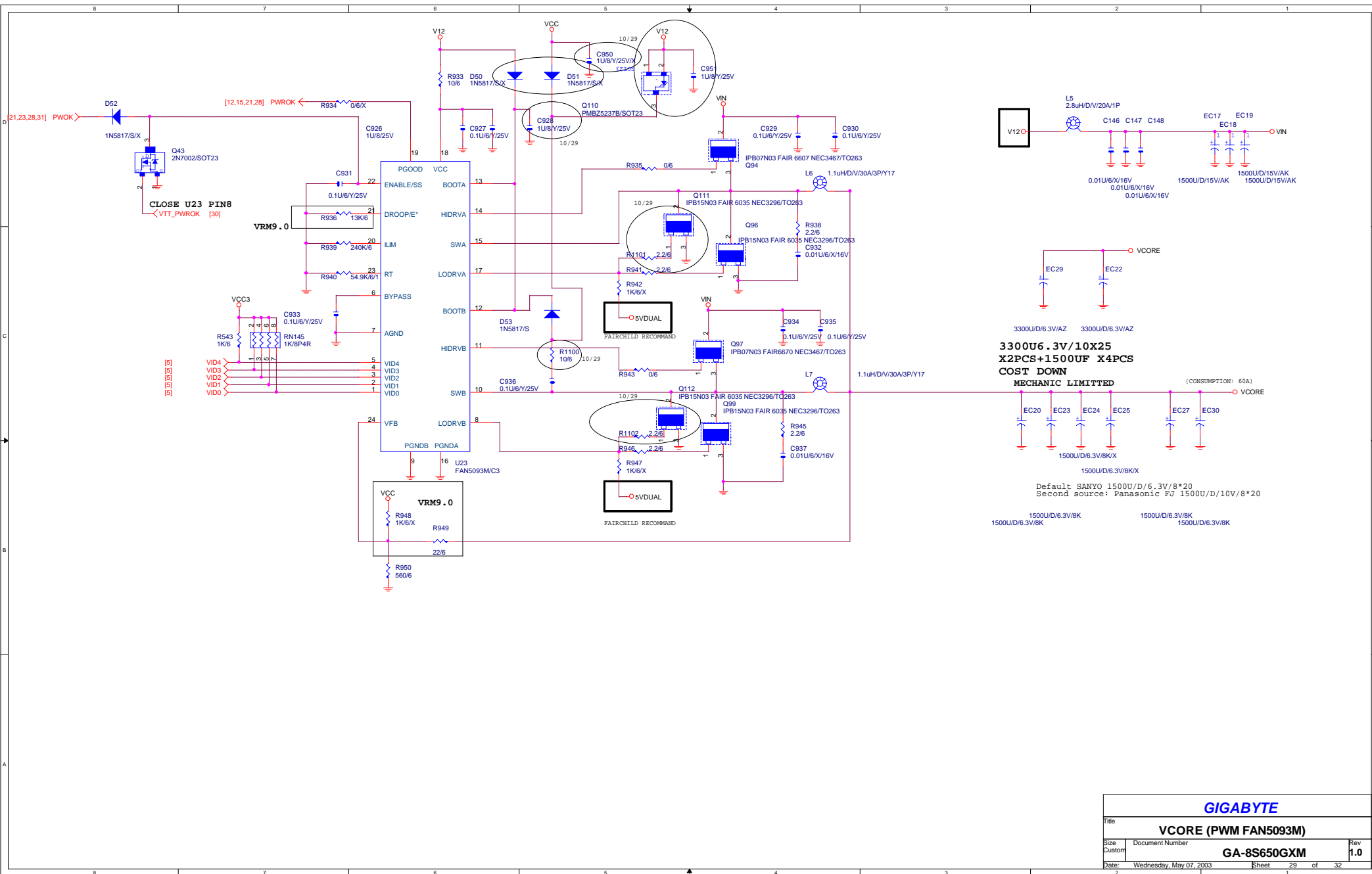
POWER FAN W=0.167W



GIGABYTE

PANEL, STR LED & FANS

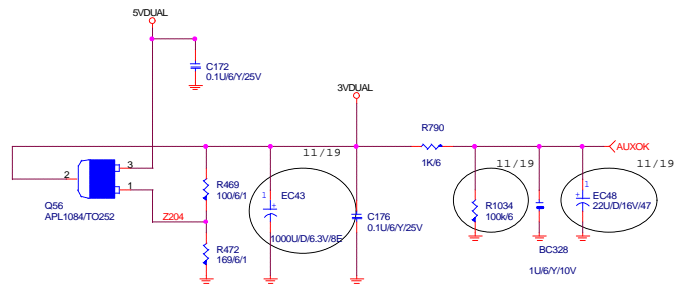
Title	Document Number	Rev
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GIGABYTE		
Title		
VCORE (PWM FAN5093M)		
Size	Document Number	Rev
Custom	GA-8S650GXM	1.0
Date	Wednesday, May 07, 2003	Sheet 29 of 32

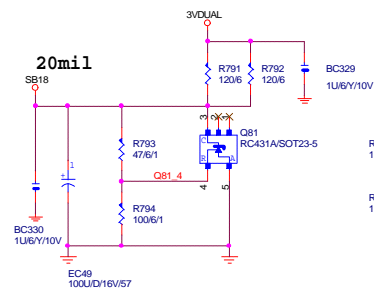
5VDUAL TRANS TO 3VDUAL(3.3V)

5VDUAL 80 mils ABOVE

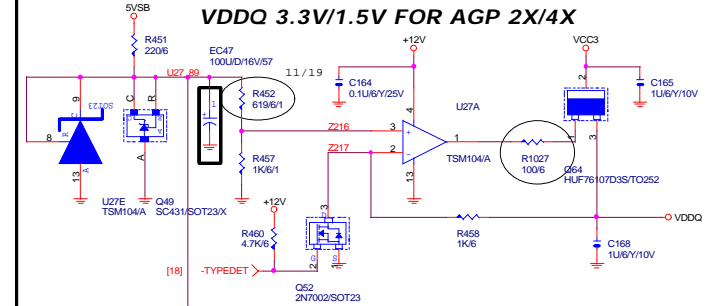


SB18 FOR SB

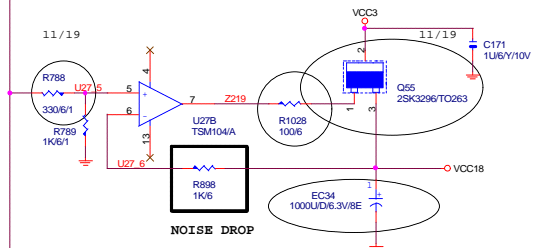
20mil



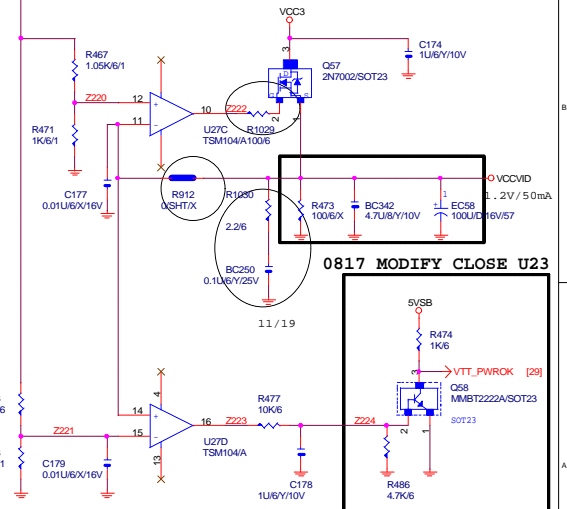
VDDQ 3.3V/1.5V FOR AGP 2X/4X



VCC18 FOR NB,SB



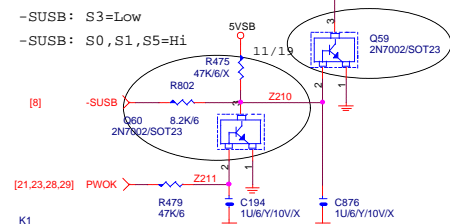
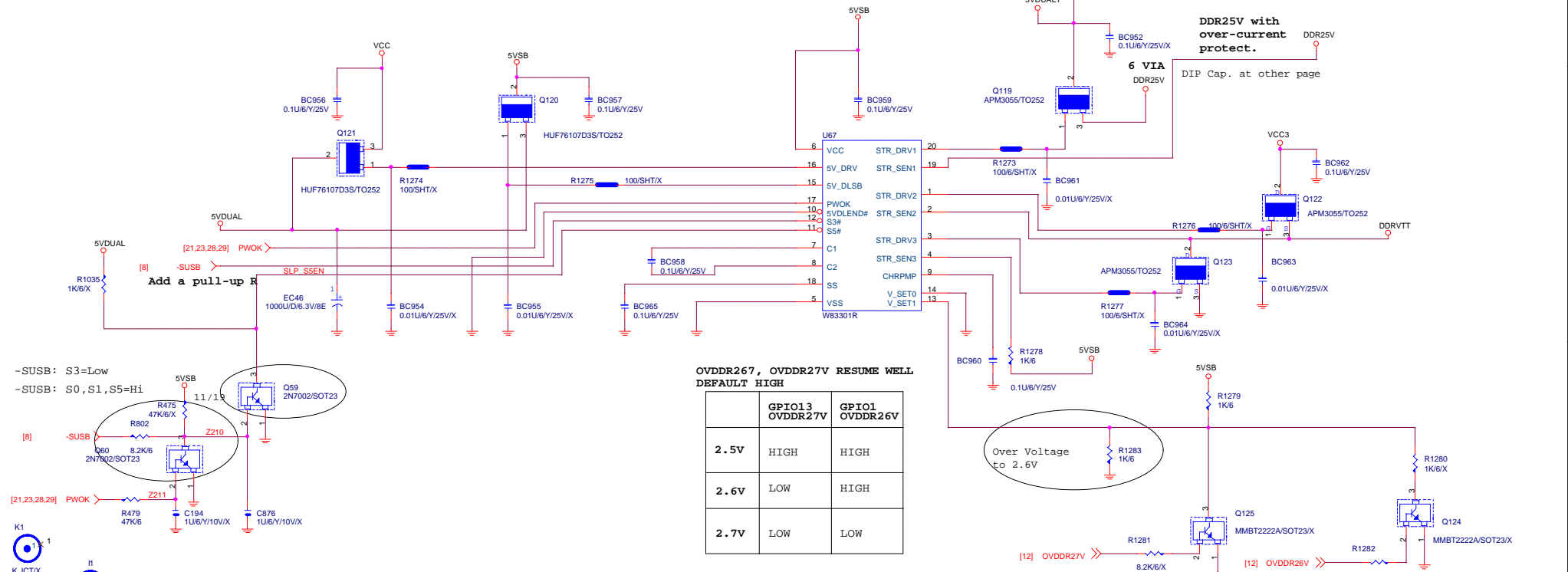
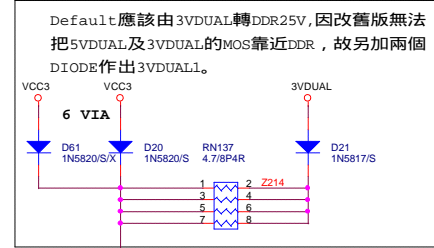
VCCVID FOR NORTHWOOD CPU



GIGABYTE		
DC POWER		
Size	Document Number	Rev
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Date:	Wednesday, May 07, 2003	Sheet 30 of 32

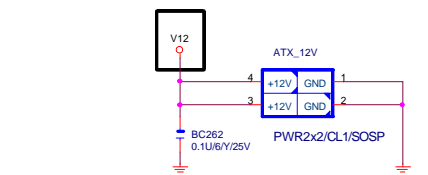
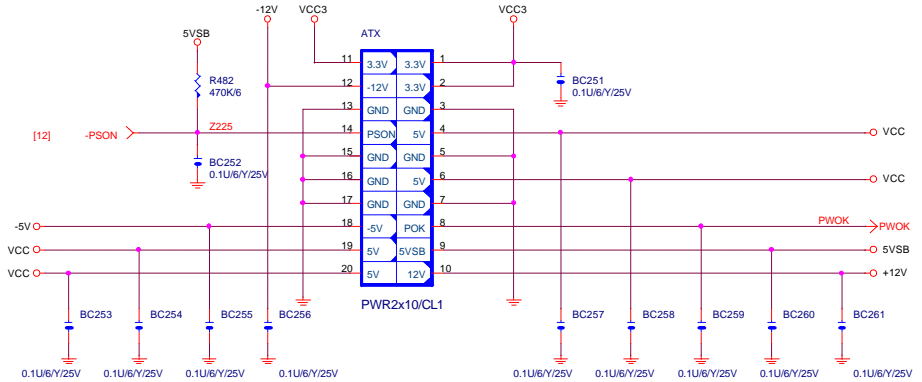
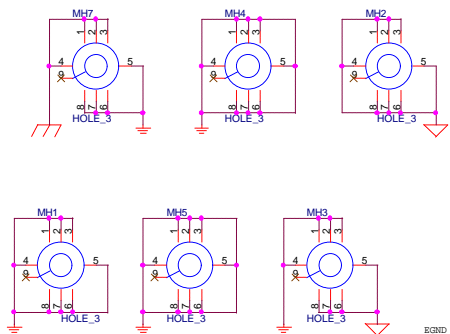
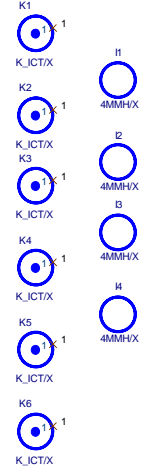
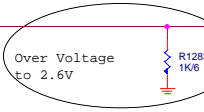
ATX CON, DDR POWER

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OVDDR267, OVDDR27V RESUME WELL DEFAULT HIGH

	GPIO13 OVDDR27V	GPIO1 OVDDR26V
2.5V	HIGH	HIGH
2.6V	LOW	HIGH
2.7V	LOW	LOW



PB REQUEST V12
+12V TRACE
250MIL

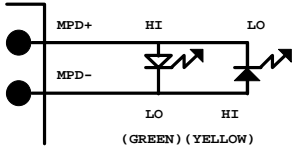
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GIGABYTE		
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ATX POWER CONNECTOR

LO:Normal

RTL8100L ON-BOARD			
-REQ0	PCI1	IDSEL(A20)--B	
-REQ1	PCI2	IDSEL(A22)--C	
-REQ2	PCI3	IDSEL(A24)--D	
-REQ3	RTL8100L	IDSEL(A27)--B	

8SRXL South Bridge GPIO LIST					
ITEM	DESCRIPTION	I/O	STATUS	Default	
GPIO0	Bios Write Protect	O	Hi:Write Enable, Lo:Write Protect	Hi	
GPIO1	N/A		PULL-UP	Hi	
GPIO2	THERM#			Hi	
GPIO3	Green Button	O	Hi:Normal, Lo:Into Green mode	Hi	
GPIO4	CLKRUN#		PULL-DOWN	Lo	
GPIO5	N/A		PULL-UP	Hi	
GPIO6	DDR OVER VOLTAGE	O		Hi	
GPIO7	SUSLED	O	AS LIKE DEFINED...	Lo	
GPIO8	Wake On Ring	I	Hi:Normal, Lo:Ring Power On	Hi	
GPIO9	GLED	I	AS LIKE DEFINED...	Lo	
GPIO10	Mother Board ID	I	SIS DEMO B/D PULL-DOWN	Lo	
GPIO11	N/A		PULL-UP	Hi	
GPIO12	N/A		PULL-UP	Hi	
GPIO13	Mother Board ID	I	SIS DEMO B/D PULL-DOWN	Lo	
GPIO14	DDR OVER VOLTAGE	I		Lo	
GPIO15	KB Data	I/OD			
GPIO16	KB Clk	I/OD			
GPIO17	MS Data	I/OD			
GPIO18	MS Clk	I/OD			



States for a single-color power LED

LED States	ACPI States	MPD+	MPD-	BIOS	
				GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING

States for a dual-color power LED

LED States	ACPI States	MPD+	MPD-	BIOS	
				GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING
Steady Yellow	S1,S3	LO	HI	HI	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING	HI	BLINKING

States for green LED

LED States	ACPI States	GLED-	BIOS
			GPIO9
ON	S1,S3	HI	HI
OFF	S0,S5	LO	LO

BIOS REQUEST

SINGLE	DUAL	INTEL LED DEFINED				GIGABYTE LED DEFINED				SINGLE	DUAL
		GPIO7	ACPILED	GPIO9		GPIO7	ACPILED	GPIO9			
GREEN	GREEN	S0	LO	LO	LO	S0	LO	LO	LO	GREEN	GREEN
OFF	YELLOW	S1	HI	HI	HI	S1	LO	BLINKING	HI	G(BLINK)	G(BLINK)
OFF	YELLOW	S3	HI	HI	HI	S3	HI	HI	HI	OFF	YELLOW
OFF	OFF	S4/S5	LO	HI/NC	LO	S4/S5	LO	HI/NC	LO	OFF	OFF

GIGABYTE

Title			
GPIO, REQ/GNT Table			
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